

PATENT
5298-04700/PM00028

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Gilboa et al.

Serial No.: 09/846,119

Filed: April 30, 2001

For: METHOD OF MAKING A
PLANARIZED SEMICONDUCTOR
STRUCTURE

Group Art Unit: 1763

Examiner: Goudreau, G.

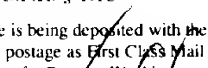
Atty. Dkt. No.: 5298-04700

CERTIFICATE OF MAILING
37 C.F.R. § 1.18

I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on the date indicated below.

9-19-03

Date



Kevin L. Daffer

DECLARATION UNDER 37 C.F.R. § 1.131

Commissioner for Patents
Washington, D.C. 20231

I, William W.C. Koutny, Jr., hereby declare and state that:

1. I am a named inventor in the above-identified patent application, which is U.S. Patent Application No. 09/846,119, filed on April 30, 2001.
2. I have been informed that in the present application, certain claims have been rejected on reference to an article in *Solid State Technology* entitled Improved Planarization for STI with Fixed Abrasive Technology by Vo et al., which was published in June of 2000.

CONCEPTION

3. As supported below, I, along with Yitzhak Gilboa, Steven Hedayati and Krishnaswamy Ramkumar, conceived of the subject matter claimed in the present application within the United States before June of 2000. The subject matter includes a method for forming a structure within a trench of a semiconductor topography.

4. Exhibit A attached hereto is a true copy of an invention disclosure form and attached pages which bear dates before June of 2000 corresponding to the conception of the invention. The actual dates for the first drawings, the first written description and first oral disclosure to others have been redacted.

5. Page 5 of Exhibit A describes the subject matter of the presently claimed case including the use of fixed abrasive polishing techniques to produce structures with a limited amount of dishing.

6. Exhibit B attached hereto is a true copy of a written description of the conceived subject matter, dated before June of 2000.


7. Page 2 of Exhibit B describes the subject matter of the rejected claims including the use of fixed abrasive polishing techniques to polish a layer deposited within a trench.

REDUCTION TO PRACTICE AND DILIGENCE

8. From at least a time just prior to June of 2000 through the filing of the application on April 30, 2001, plans were undertaken to prepare the captioned patent application, which was commissioned to Kevin Daffer at Conley, Rose & Tayon, P.C. I did not abandon, suppress, or conceal the ideas set forth in the claimed invention during at least the time beginning just prior to June of 2000 through the filing of the application on April 30, 2001.

9. Upon information and belief, it is my informed understanding that diligence in reducing the invention to practice was therefore maintained from at least as early as just prior to June of 2000 through the filing of the application on April 30, 2001.

10. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.



William W.C. Koutny, Jr.

Date: 7/10/03

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

1. INVENTOR(S)

DISCLOSURE NO PM00028

A. Name YITZHAK GILSON CY Initials YEG Empl. No. 73035 Ext. No. 2719
 Citizenship USA Dept # UCP Home Phone No. UCP-253-8307
 Home Mailing Address 1761 HERMAN AVE SAN MARINO, CA 91027

B. Name William Gregory CY Initials BIS Empl. No. 135 Ext. No. 2613
 Citizenship USA Dept # Home Phone No. 408-247-0565
 Home Mailing Address 7555 Homestead #45 San Jose, CA 95051
2555 Homestead #5 95051

C. Name Steven Hedgcock CY Initials SSH Empl. No. 8534 Ext. No. 4556
 Citizenship USA Dept # 3103 Home Phone No. 408-927-9187
 Home Mailing Address 1240 Valley View Circle San Jose CA 95120

2. TITLE OF INVENTION Method of making shallow trench isolation structure

3. CONCEPTION OF INVENTION

A. Date of first drawing or drawings Redacted
 Where can first drawing be found Redacted
 B. Date of first written description Redacted
 Where is description found Redacted
 C. Date of first oral disclosure to others Redacted
 To whom? discussed with KTH, SSH, BIS

4. CONSTRUCTION OF DEVICE

A. Date Completed
 B. Was prototype made?
 C. By whom made?
 D. Where can the prototype be found?

Inventor(s): <u>William Gregory</u>	Date: <u>7/24/80</u>
Inventor(s): <u>Steven Hedgcock</u>	Date: <u>8/24/80</u>
Inventor(s): <u>Yitzhak Gilson</u>	Date: <u>8/24/80</u>
Witnessed, Read, and Understood by: <u>[Signature]</u>	Date: <u>8/24/80</u>
Witnessed, Read, and Understood by: <u>U. G. [Signature]</u>	Date: <u>8/24/80</u>

Each page upon which information is entered should be signed and witnessed.

Exhibit A - page 1

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

1. INVENTOR(S)

DISCLOSURE NO. _____

A. Name Ramkumar CY Initials KTR Empl. No. 3305 Ext. No. 2720
Citizenship INDIAN Dept # 3108 Home Phone No. (408) 255-1031
Home Mailing Address 1193 LYNBROOK WAY, SAN JOSE, CA 95128

B. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____
Citizenship _____ Dept # _____ Home Phone No. _____
Home Mailing Address _____

C. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____
Citizenship _____ Dept # _____ Home Phone No. _____
Home Mailing Address _____

2. TITLE OF INVENTION _____

3. CONCEPTION OF INVENTION

- A. Date of first drawing or drawings _____
Where can first drawing be found _____
- B. Date of first written description _____
Where is description found _____
- C. Date of first oral disclosure to others _____
To whom? _____

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- C. By whom made? _____
- D. Where can the prototype be found? _____

Inventor(s): _____ Date _____

Inventor(s): _____ Date _____

Inventor(s): _____ Date _____

Witnessed, Read, and Understood by: _____ Date _____

Witnessed, Read, and Understood by: _____ Date _____

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CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

5. TEST OF DEVICE

A. Date: _____ Witness(es): _____

B. Results: _____

6. SALE

A. Was invention sold or offered for sale? Yes No ☒

B. Was invention used to make, assemble or test a commercial product? Yes No ☒

C. Will invention be sold, offered for sale, sampled, or used to make, assemble or test a commercial product? Yes No ☒

D. Actual or estimated date of first sale, offer or commercial use

E. Is invention part of a product for which there is a data sheet? Yes ☐ No ☒ (If yes, attach a copy)

F. Actual or estimated date of publication, release or availability of data sheet

7. USE

A. Is invention presently being used? Yes No ☒

B. In what product or process is invention presently being used?

Are there specific plans for its use in near future? In what products or processes?

RAM-P

8. RELATED PRINTED PUBLICATIONS, PATENTS, PATENT APPLICATIONS

5,972,792 / 4010533 / 5782675 / 5919072

9. **WAS INVENTION** Conceived (Yes _____ (No 1 /) Constructed (Yes _____ (No 1 /) Tested (Yes _____ (No 1 /) during performance of Government Contract?

Contract Number _____
(Give Full Contract Number)

The description of invention should be written in the inventor's own words and generally should follow the outline given below. Sketches, prints, photos, and other illustrations, as well as memos or reports of any

Inventory: Walter H. H. H. Date 7-2-50

Inventory: S. H. Marsh Date 6/20/60

Inventory: *[Signature]* Date: *07-24-07*

Witnessed, Read, and Understood by: [Signature] Date: 2-20-94

Witnessed, Read, and Understood by ASL Date 8/24/88

Each page upon which information is entered should be signed and witnessed.

Exhibit A - page 3

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

FOR ANSWERS TO THE FOLLOWING QUESTIONS, USE THE REMAINDER OF SHEET AND THE ATTACHED SHEET(S).

1. General purpose of invention. State in general terms the objects of the invention.
 2. Describe old technology, if any, for performing the function of the invention. Provide references, if available.
 3. Indicate the disadvantages of the old technology.
 4. Describe your invention and its construction, showing the changes, additions and improvements over the old method.
 5. Give details of its operation (i.e., how is your invention used?), if not already described under 4.
 6. State the advantages of your invention over what has been done before.
 7. Indicate any alternate component(s) and/or method(s) of construction.
 8. If a joint invention, indicate what contribution was made by each inventor.
 9. Describe the features that are believed to be new.
 10. State opinion of relative value of invention.
- ***
11. After the disclosure is prepared, it should be signed by the inventor(s) and then read and signed by two witnesses in the space provided at the bottom of each sheet. Forward an electronic copy of this form, as well as a paper copy bearing original signatures, to the Intellectual Property Department.

d. The purpose of the invention is to improve the manufacturability of STI and reduce cost, to be done by reducing processing steps.

2. Current technology (27-30 TPa) calls for the following steps:

$\frac{1}{2} \times 2 = 1$ $\frac{1}{2} \times 2 = 1$ $\frac{1}{2} \times 2 = 1$ $\frac{1}{2} \times 2 = 1$ $\frac{1}{2} \times 2 = 1$

Inventor's: William H. Smith Date 5/24/80

Inventor(s) J. H. Smith Date 8/24/00

Inventor(s) W. B. C. Date 2-24-40

Witnessed Read and Understood By: [Signature] Date 8/29/50

Witnessed, Read, and Understood by: M. Sadik Date 5/24/73

Each page upon which information is entered should be signed and witnessed.

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

nature in which the invention is referred to, if available, should form a part of this disclosure and reference can be made thereto in the descriptions of the invention's construction and operation.

(3) Disadvantages addressed by invention:

1. Thick nitride - layer required to overcome sputtering in etching process. This nitride can include stress defects.
2. Additional etch required to etch nitride.
3. Etch stop after nitride etch which can result in side stringing.
4. Thicker oxide fill deposition to overcome etch induced by nitride.

(4) The current invention has three options as using Fixed Abrasive pattern as the ~~main~~ method of etching. The main advantage of Fixed Abrasive is the negligible amount of stringing compared to conventional etching processes. The second advantage is self planarization. Both note resources at file.

Option I - No Nitride Hard mask.

In this option, no nitride is used. Etching is done on base oxide. Trench etch is done as if one step is etching. The trench is opened. After trench etch, oxide fill is done in the trench and across the contacts a thickness of the trench + trench depth variation. After oxide deposition the oxide is polished using Fixed Abrasive to a residual thickness of 0-500 Å. The last two processes are self planarization and self cleaning. The etch is done in a single step.

Inventor(s):	<u>James H. Smith</u>	Date:	<u>8-22-80</u>
Inventor(s):	<u>J. H. Smith</u>	Date:	<u>8-22-80</u>
Inventor(s):	<u>J. H. Smith</u>	Date:	<u>8-22-80</u>
Witnessed, Read and Understood by:	<u>[Signature]</u>	Date:	<u>8-22-80</u>
Witnessed, Read and Understood by:	<u>[Signature]</u>	Date:	<u>8-22-80</u>

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CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

Option II - Deposit Thin Altrid -

grow base oxide grow thin layer of Altrid (0-500Å)
 expose Field oxide mask, Etch remove, Deposit fill oxide
 polish down to ~~Altrid~~ stop on oxide at a predetermined
 Residual oxide above the Altrid. Strip remaining oxide.
 Strip remaining Altrid.

Option III

grow base oxide deposit $FeSi_2/PSG$, expose field
 Etch trench, deposit Si_3N_4 oxide, polish to PSG/PSG layer
 use wet strip to remove remaining $FeSi_2$, use debulked
 wet strip to remove oxide, Due to wet Etch Rate
 differences of $FeSi_2$ to remaining oxide this will
 result in positive step of isolation, carry Anneal 50.

⑥ - Two drawings of silicon properties of each invention
 showing the use of each in a specific device.

⑦ - Drawings of a new device using each invention showing a
 new use of each invention.

Inventor(s):	<u>William Murphy</u>	Date:	<u>3/24/80</u>
Inventor(s):	<u>J. Hedgcock</u>	Date:	<u>3/24/80</u>
Inventor(s):	<u>[Signature]</u>	Date:	<u>3/24/80</u>
Witnessed, Read, and Understood by:	<u>[Signature]</u>	Date:	<u>3/26/80</u>
Witnessed, Read, and Understood by:	<u>[Signature]</u>	Date:	<u>3/24/80</u>

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Exhibit A - page 6

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

- (8) equal contribution
- (9) Fixed abrasive polish, no polish step, different Polish steps
- (10) - Invention will enable reduction of cost of ownership compared to Sony.
 - enable 5th polish without requirement of reverse wash.
 - enable 5th polish with reduced step height budget required for 143 nm lithography.

Inventor(s) M. J. H. H. H. H. H. Date 0-0-00

Inventor(s) J. McDonald Date 5/28/01

Inventor(s) John J. ... Date 12-1-77

Witnessed, Read, and Understood by: [Signature] Date Aug 1980

Witnessed, Read, and Understood by: E. J. 32 Date 8/24/20

Each page upon which information is entered should be signed and witnessed.



Option 1

- No Nitride IIM
- Stop after flatness - fixed abrasive
- Wet dip to below Si

CMP →

HF dip →

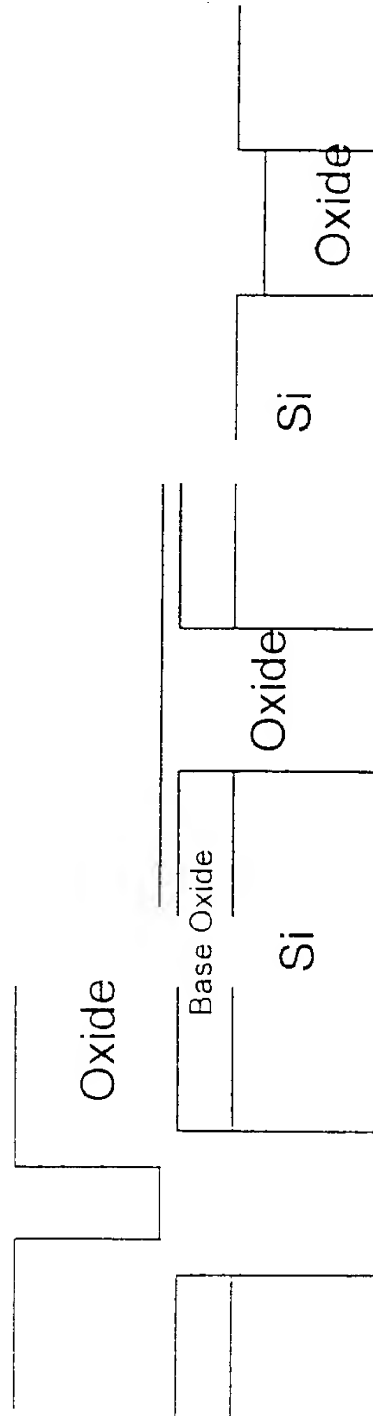


Exhibit A- page 8



CYPRESS

STI Invention Disclosure

Method of Making STI

Option 1

WD4
W: #03

24-AUG-00
dense

Depth 43nm

10.0kV X80.0k 375nm

WD5
W: #01

25-AUG-00

**X : 0.00nm
**D : 0.00nm

10.0kV X80.0k 375nm

Exhibit A- page 9



CYPRESS

STI Invention Disclosure

Option 2

- Use doped oxide to increase selectivity during wet Dip
- polish to flatness - Fixed Abrasive
- Wet dip - ratio of doped oxide thickness to un-doped thickness controls step height

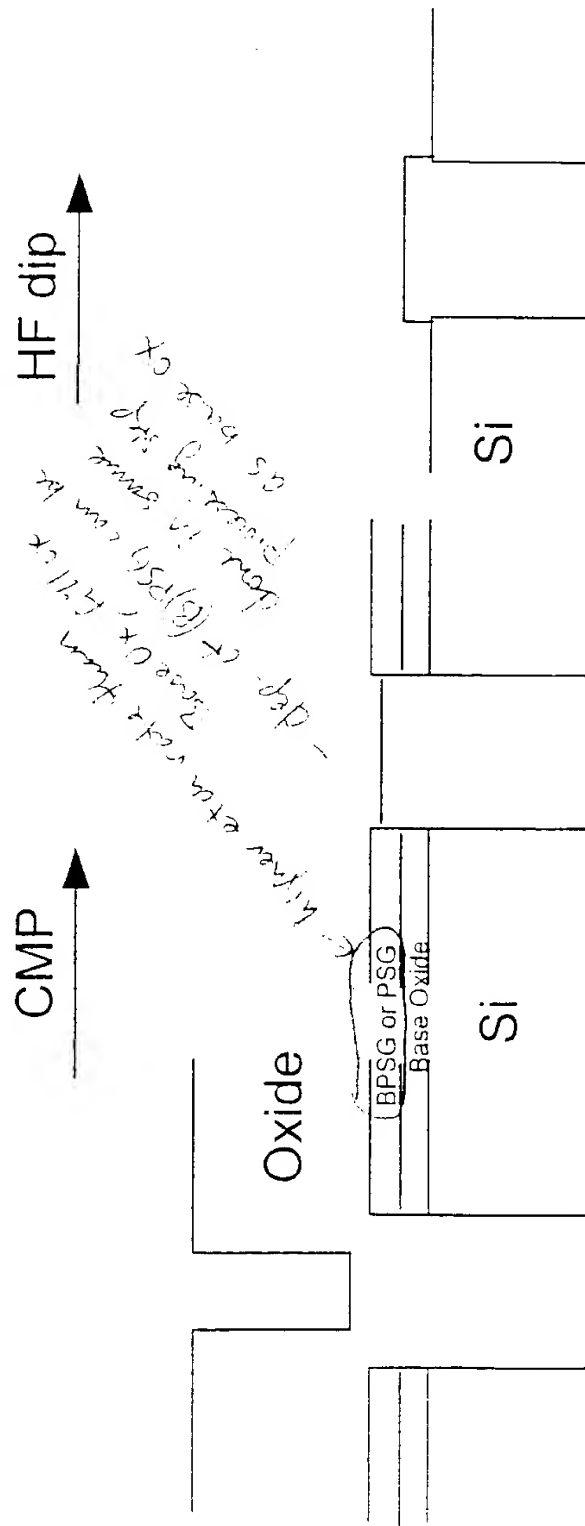


Exhibit A - page 10



CYPRESS

STI Invention Disclosure

Option 3

*Use thin Nitride
polish to flatness (nitride) to
determine the step height and not as polish stop*

- Use thin Nitride
- polish to flatness - Fixed Abrasive, stop with oxide over Nitride, nitride is used to determine the step height and not as polish stop.
- Wet dip - Nitride thickness controls step height

CMP

HF dip + Nitride Strip

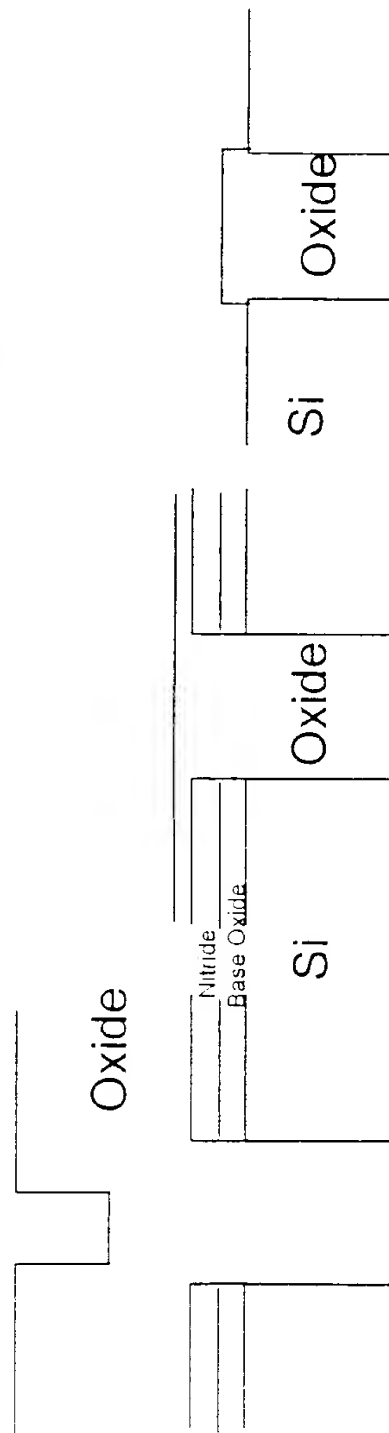
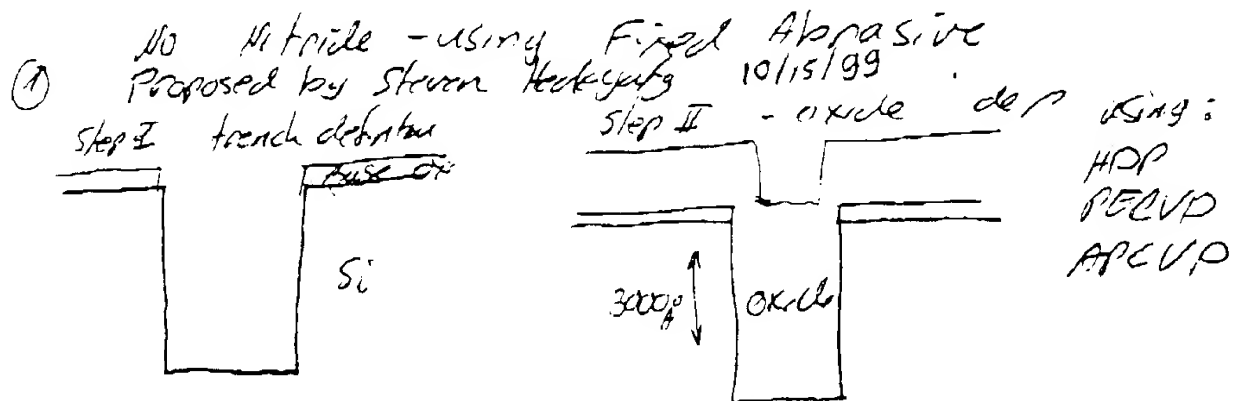


Exhibit A - page 11

STC

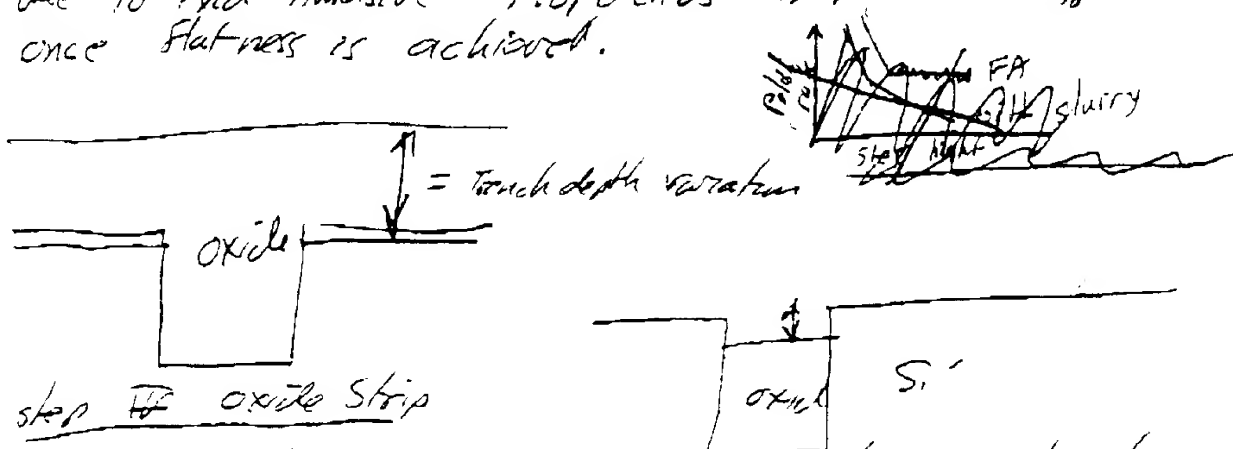
method of making shallow trench isolation
structure with no/or thin nitride cap step.



in step II
need to deposit trench depth + trench depth variation

step II polish

due to Fixed Abrasive properties CMP will self planarize
once flatness is achieved.



strip? will result in oxide below Si level

Steven Hegarty, Rombur, Bill Kating, Mike Allen

S. Hegarty

A. Blosie

11/15/99

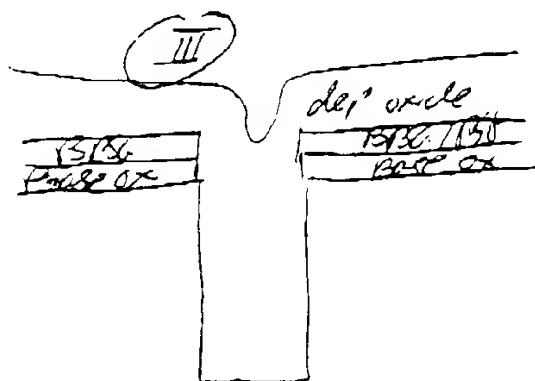
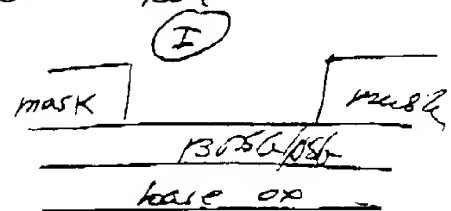
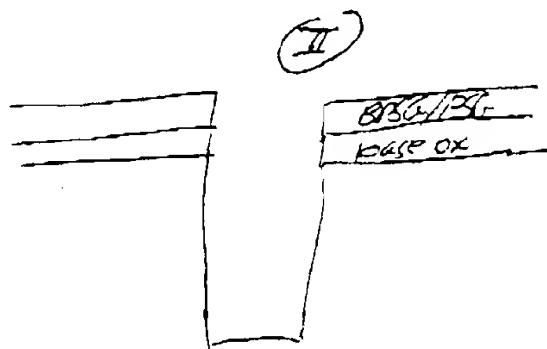
11/15/99

Exhibit B - page 1

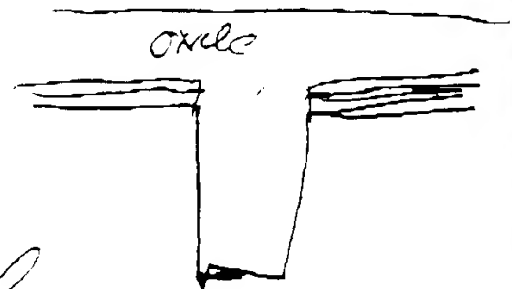
STC

as long as trench depth variation is controlled below a certain number ie ± 500 Å then polish can be done without ~~the~~ nitride layer.

② 2nd method use of polysilicon layer as a base oxide or on top of base oxide



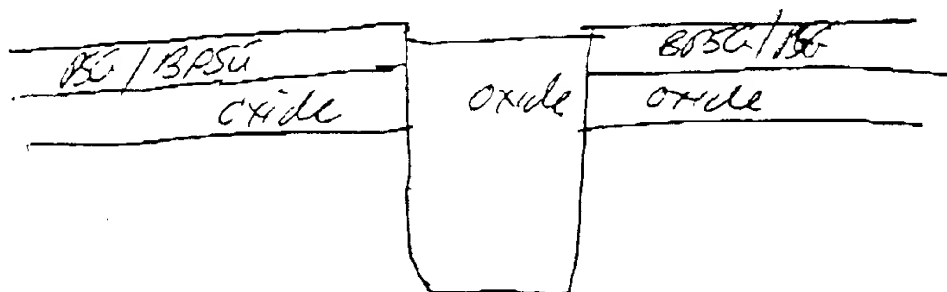
Polish using Final Abrasive



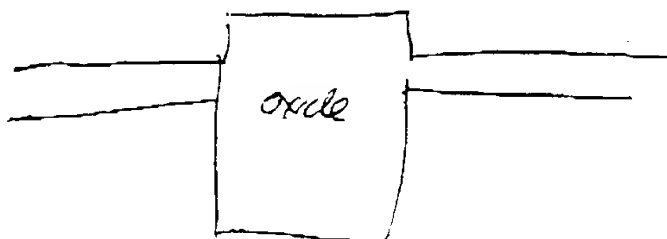
Bill Koutney
S. Hedge
Alan B. Bore

11/15/89
11/15/99

~~strip oxide back to BPSG~~
 Polish Back to BPSG layer
 strip



use wet strip BPSG ER is ~50 times
 thermal oxide rate so result will be
 after strip I



after strip II



Bill Koutney 1/26 C. L. Lee
 J. Hedgcock
 Dr. C. L. Lee

11/15/99
 11/15/99

Exhibit B- page 3

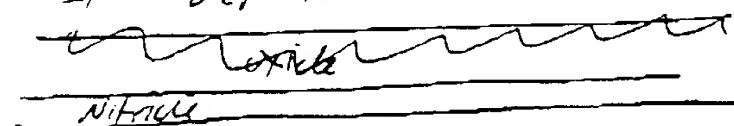
Si

(3)

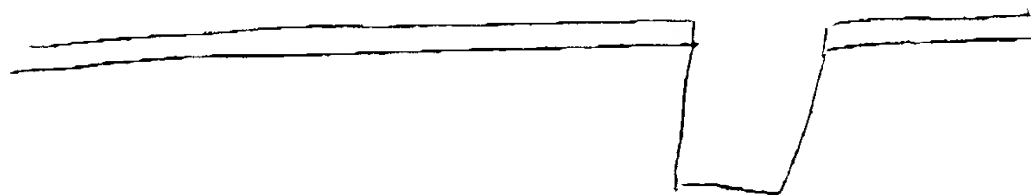
use thin Nitride for Si

Nitride is used only as a means
to determine oxide height above Si

I dep thin Nitride

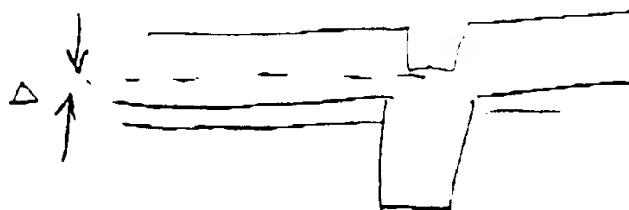


II mask and etch



III

dep HPS oxide or PECVD oxide or APCVD
oxide



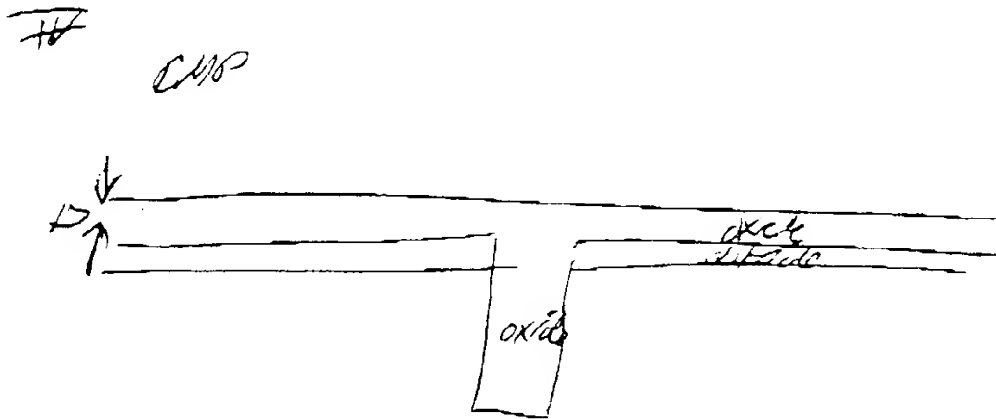
Thickness is
targeted to
achieve planarity
at ΔA above

Si

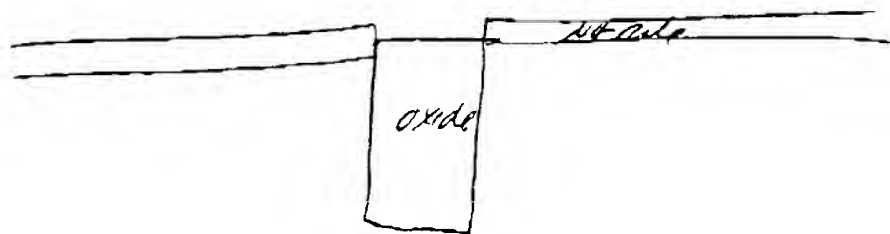
Bill Kaufman - 1/16/99
J. Hedger
Alan Bloome

11/15/99 -
11/15/99 -

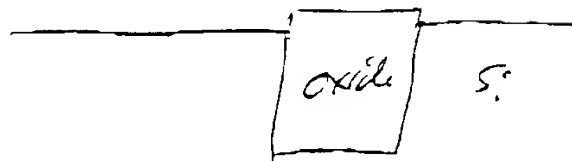
Exhibit B- page 4



V wet strip of oxide



VI pure strip



Bill Kennedy 1/16/66
 S. Hedgcock
 Alan Blum

10/15/89
 10/15/99



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For: METHOD OF MAKING A
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STRUCTURE

Group Art Unit: 1763

Examiner: Goudreau, G.

Atty. Dkt. No.: 5298-04700

RECEIVED
SEP 30 2003
TC 1700

CERTIFICATE OF MAILING
37 C.F.R. § 1.18

I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on the date indicated below.

Date

Kevin L. Daffer

DECLARATION UNDER 37 C.F.R. § 1.131

Commissioner for Patents
Washington, D.C. 20231

I, Steven Hedayati, hereby declare and state that:

1. I am a named inventor in the above-identified patent application, which is U.S. Patent Application No. 09/846,119, filed on April 30, 2001.

2. I have been informed that in the present application, certain claims have been rejected on reference to an article in *Solid State Technology* entitled Improved Planarization for STI with Fixed Abrasive Technology by Vo et al., which was published in June of 2000.

RECEIVED

SEP 28

OFFICE OF PETITIONS

CONCEPTION

3. As supported below, I, along with Yitzhak Gilboa, William W.C. Koutny, Jr. and Krishnaswamy Ramkumar, conceived of the subject matter claimed in the present application within the United States before June of 2000. The subject matter includes a method for forming a structure within a trench of a semiconductor topography.

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8. From at least a time just prior to June of 2000 through the filing of the application on April 30, 2001, plans were undertaken to prepare the captioned patent application, which was commissioned to Kevin Daffer at Conley, Rose & Tayon, P.C. I did not abandon, suppress, or conceal the ideas set forth in the claimed invention during at least the time beginning just prior to June of 2000 through the filing of the application on April 30, 2001.

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Steven Hedayati

Date: _____

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

1. INVENTOR(S)

DISCLOSURE NO PM00028

A. Name YITZHAK GOLDBA CY Initials YEG Empl. No. 7395 Ext. No. 2719
 Citizenship USA Dept # 208 Home Phone No. 408-2538867
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 Citizenship US Dept # Home Phone No. 408-247-0525
 Home Mailing Address 7555 Homestead #45 Santa Clara, CA 95051
2555 Homestead #5 95051

C. Name Steven Hedyati CY Initials SSH Empl. No. 8584 Ext. No. 4556
 Citizenship US Dept # 3108 Home Phone No. 408-927-9187
 Home Mailing Address 1240 Valley Quail Circle San Jose CA 95120

2. TITLE OF INVENTION Method of making shallow trench isolation structure

3. CONCEPTION OF INVENTION

A. Date of first drawing or drawings Redacted
 Where can first drawing be found Redacted
 B. Date of first written description Redacted
 Where is description found Redacted
 C. Date of first oral disclosure to others Redacted
 To whom? discussed with KTR, SS, BK

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A. Date Completed
 B. Was prototype made?
 C. By whom made?
 D. Where can the prototype be found?

Inventor(s) <u>William Hartney</u>	Date <u>8/24/00</u>
Inventor(s) <u>S. Hedyati</u>	Date <u>8/24/00</u>
Inventor(s) <u>Y. Goldba</u>	Date <u>8/24/00</u>
Witnessed, Read, and Understood by: <u>[Signature]</u>	Date <u>8/24/00</u>
Witnessed, Read, and Understood by: <u>[Signature]</u>	Date <u>8/24/00</u>

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1. INVENTOR(S)

DISCLOSURE NO. _____

A. Name Ramkumar CY Initials KTR Empl. No. 3305 Ext. No. 2720
Citizenship INDIAN Dept # 3108 Home Phone No. (408) 255-1031
Home Mailing Address 1193 LYNBROOK WAY ; SAN JOSE ; CA 95128

B. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____
Citizenship _____ Dept # _____ Home Phone No. _____
Home Mailing Address _____

C. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____
Citizenship _____ Dept # _____ Home Phone No. _____
Home Mailing Address _____

2. TITLE OF INVENTION _____

3. CONCEPTION OF INVENTION

A. Date of first drawing or drawings _____
Where can first drawing be found _____
B. Date of first written description _____
Where is description found _____
C. Date of first oral disclosure to others _____
To whom? _____

4. CONSTRUCTION OF DEVICE

A. Date Completed _____
B. Was prototype made? _____
C. By whom made? _____
D. Where can the prototype be found? _____

Inventor(s): _____ Date _____

Inventor(s): _____ Date _____

Inventor(s): _____ Date _____

Witnessed, Read, and Understood by: _____ Date _____

Witnessed, Read, and Understood by: _____ Date _____

Each page upon which information is entered should be signed and witnessed

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

5. TEST OF DEVICE

A. Date: _____ Witness(es): _____

B. Results: _____

6. SALE

A. Was invention sold or offered for sale? Yes ☐ No ☒

B. Was invention used to make, assemble or test a commercial product? Yes ☐ No ☒

C. Will invention be sold, offered for sale, sampled, or used to make, assemble or test a commercial product? Yes ☐ No ☒

D. Actual or estimated date of first sale, offer or commercial use

E. Is invention part of a product for which there is a data sheet? Yes ☐ No ☒ (If yes, attach a copy)

F. Actual or estimated date of publication, release or availability of data sheet

7. USE

A. Is invention presently being used? Yes ☐ No ☒

★ ★ ★

B. In what product or process is invention presently being used?

Are there specific plans for its use in near future? In what products or processes?

RAM-P

8. RELATED PRINTED PUBLICATIONS, PATENTS, PATENT APPLICATIONS

5,972,792 / 4010533 ~~4010533~~ 5,782,675 / 5919082
4393627 / ~~4393627~~

9. **WAS INVENTION** Conceived (Yes ☐ (No ☒ Constructed (Yes ☐ (No ☒ Tested (Yes ☐ (No ☒ during performance of Government Contract?

Contract Number _____
(Give Full Contract Number)

The description of invention should be written in the inventor's own words and generally should follow the outline given below. Sketches, prints, photos, and other illustrations, as well as memos or reports of any

Inventor(s) Walter Smith Date 5/2/2006

Inventor(s) S. H. Kural / 1 / 1 Date 9/20/00

Inventor(s) 0 1/4 1/2 Date 11/24/0

Witnessed, Read, and Understood by: [Signature] Date 5/26/00

Witnessed, Read, and Understood by: H. S. [Signature] Date 8/24/63

Each page upon which information is entered should be signed and witnessed.

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

FOR ANSWERS TO THE FOLLOWING QUESTIONS, USE THE REMAINDER OF SHEET AND THE ATTACHED SHEET(S).

1. General purpose of invention. State in general terms the objects of the invention.
 2. Describe old technology, if any, for performing the function of the invention. Provide references, if available
 3. Indicate the disadvantages of the old technology.
 4. Describe your invention and its construction, showing the changes, additions and improvements over the old method
 5. Give details of its operation (i.e., how is your invention used?), if not already described under 4.
 6. State the advantages of your invention over what has been done before.
 7. Indicate any alternate component(s) and/or method(s) of construction.
 8. If a joint invention, indicate what contribution was made by each inventor.
 9. Describe the features that are believed to be new.
 10. State opinion of relative value of invention.
- ***
11. After the disclosure is prepared, it should be signed by the inventor(s) and then read and signed by two witnesses in the space provided at the bottom of each sheet. Forward an electronic copy of this form, as well as a paper copy bearing original signatures, to the Intellectual Property Department.

[illegible]

4. The purpose of the invention is to improve the manufacturability of SiT and reduce cost. This is done by reducing processing steps.

2. Current technology (R7-18 TDR) calls for the following steps:

$\text{BPR} \rightarrow \text{NOC} \rightarrow \text{FEM} \rightarrow \text{STATE} \rightarrow \text{STRE} \rightarrow \text{CURR} \rightarrow \text{FIELD} \rightarrow \text{CAPACITY}$

Inventor(s) William M. Smith Date 6-2-90

Inventor(s) J. H. Hual Date 8/24/00

Inventor(s) W. L. G. 3 Date 7-24-61

Witnessed, Read, and Understood by: [Signature] Date 8/24/00

Witnessed, Read, and Understood by: M. S. Smith Date 8/24/57

Each page upon which information is entered should be signed and witnessed

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

nature in which the invention is referred to, if available, should form a part of this disclosure and reference can be made thereto in the descriptions of the invention's construction and operation.

(3) Disadvantages addressed by invention:

1. Thick nitride - layer required to overcome SCOA etching in slurry etch process. This nitride can induce stress defects.
2. Additional etch required to Etch nitride
3. Extra step after a fab step which can result in Poly stringer
4. Thinner oxide fill deposition to overcome step induced by nitride.

- (4) The current invention has three options all using Fixed Abrasive polish as the ~~main~~ method of polish.
- The main advantage of Fixed Abrasive is the negligible amount of material compared to conventional slurry processes.
- The second advantage is self planarization since rate reduction at flat.
- Option I - no nitride hard mask

In this option no nitride hard mask. Fixed abrasive on base oxide trench area. ~~comparing~~ ^{is one step in which the trench is opened.} After trench open oxide fill is deposited in the trench and across the wafer to a thickness of the trench + trench depth variation. After oxide deposition the wafer is polished using Fixed Abrasive to a residual thickness of 0-500Å. The last step involves a wet chemical clean to remove the oxide from the Si surface in process.

Inventor's: <u>Michael M. Smith</u>	Date: <u>8/26/80</u>
Inventor's: <u>L. H. Smith</u>	Date: <u>8/26/80</u>
Inventor's: <u>John R. Smith</u>	Date: <u>8/26/80</u>
Witnessed Read and Understood by: <u>[Signature]</u>	Date: <u>8/26/80</u>
Witnessed Read and Understood by: <u>L. H. Smith</u>	Date: <u>8/26/80</u>

Each page upon which information is entered should be signed and witnessed.

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

option II - deposit thin nitride -

grow base oxide grow thin layer of nitride (0-500 Å)
 expose field oxide must etch handle, deposit fill oxide
 polish down to ~~nitride~~ stop on oxide at a predetermined
 residual oxide above the nitride. Stop remaining oxide.
 Stop remaining nitride.

option III

grow base oxide deposit BPSG, expose field
 etch trench, deposit fill oxide, polish to BPSG layer
 use wet strip to remove remaining BPSG, use defined
 wet strip to remove oxide, due to wet-etch rate
 differences of BPSG to nitride oxide film this will
 result in positive stop of nitride oxide. About 50.

- ⑥ - Using advantage of wet-etch rate of nitride oxide
 allowing the use of wet-etch to remove BPSG.
- ⑦ - Alternative to wet-etch BPSG, use regular growing a
 thick pass layer - polysilicon nitride.

Inventor(s):	<u>mm mm mm</u>	Date:	<u>8/24/85</u>
Inventor(s):	<u>J. Heimerl</u>	Date:	<u>8/24/85</u>
Inventor(s):	<u>J. Heimerl</u>	Date:	<u>8/24/85</u>
Witnessed, Read, and Understood by:	<u>[Signature]</u>	Date:	<u>8/24/85</u>
Witnessed, Read, and Understood by:	<u>[Signature]</u>	Date:	<u>8/24/85</u>

(Each page upon which information is entered should be signed and witnessed.)

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

- (8) equal contribution
- (9) Fixed Abrasive polish, no polish step, different polish steps
- (10) Invention will enable reduction of cost of ownership compared to Sony.
- enable STI polish without requirement of reverse mask.
 - enable STI polish with reduced step height budget required for 193 nm lithography.

Inventor(s) <u>William H. Lee</u>	Date <u>8/22/00</u>
Inventor(s) <u>J. Hedgcock</u>	Date <u>8/22/00</u>
Inventor(s) <u>[Signature]</u>	Date <u>8/22/00</u>
Witnessed, Read, and Understood by: <u>[Signature]</u>	Date <u>8/24/00</u>
Witnessed, Read, and Understood by: <u>[Signature]</u>	Date <u>8/24/00</u>

(Each page upon which information is entered should be signed and witnessed.)



CYPRESS

STI Invention Disclosure

Option 1

- No Nitride HM
- Stop after flatness - fixed abrasive
- Wet dip to below Si

CMP

HF dip

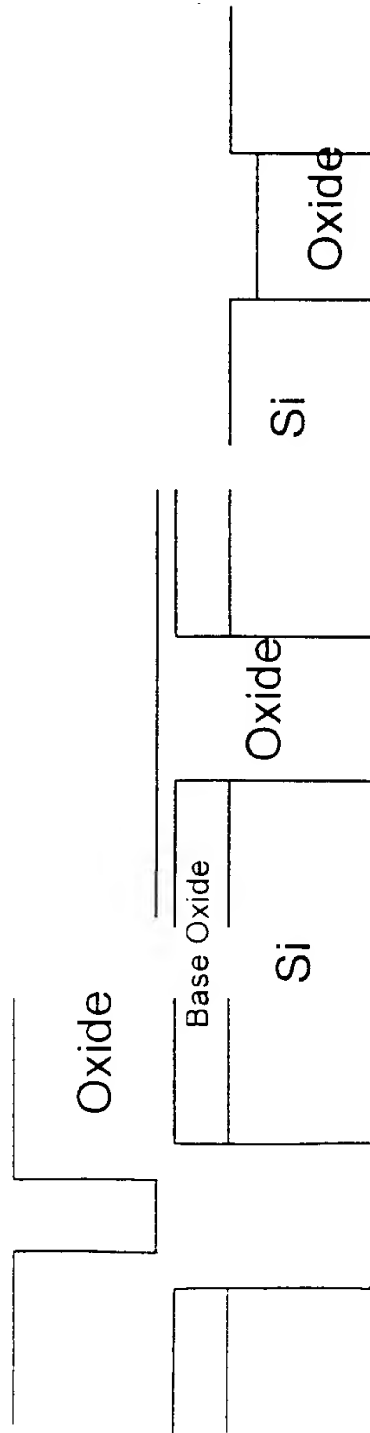


Exhibit A- page 8



CYPRESS

STI Invention Disclosure

Method of Making STI

Option 1

WD4
W.#03

24-AUG-00
dense

Depth 43nm

10.0kV X80.0K 375nm

WD5
W.#01

25-AUG-00

XY : 0.000nm
ZD : 320.0nm

10.0kV X80.0K 375nm

Exhibit A- page 9



CYPRESS

STI Invention Disclosure

Option 2

- Use doped oxide to increase selectivity during wet Dip
- polish to flatness - Fixed Abrasive
- Wet dip - ratio of doped oxide thickness to un-doped thickness controls step height

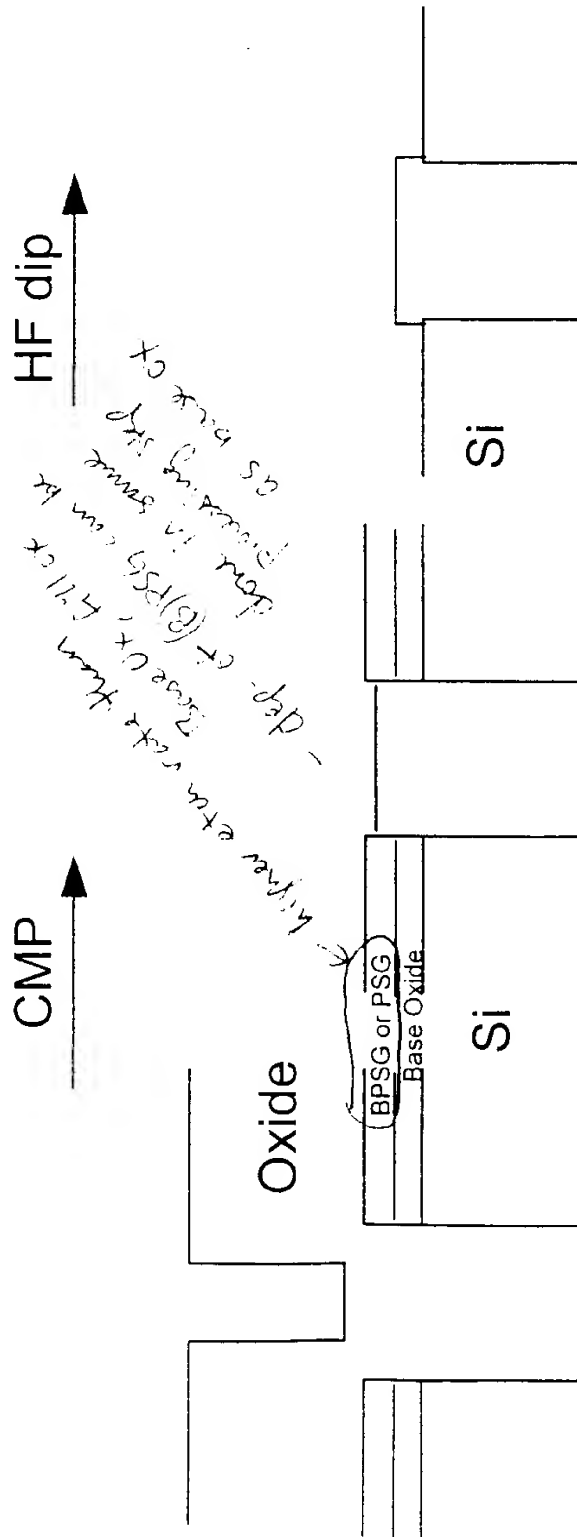


Exhibit A - page 10



CYPRESS

STI Invention Disclosure

Option 3

Use thin Nitride
polish to flatness (2000 Å) to
determine the step height and not as polish stop

- Use thin Nitride
- polish to flatness - Fixed Abrasive, stop with oxide over Nitride, nitride is used to determine the step height and not as polish stop.
- Wet dip - Nitride thickness controls step height

CMP

HF dip + Nitride Strip

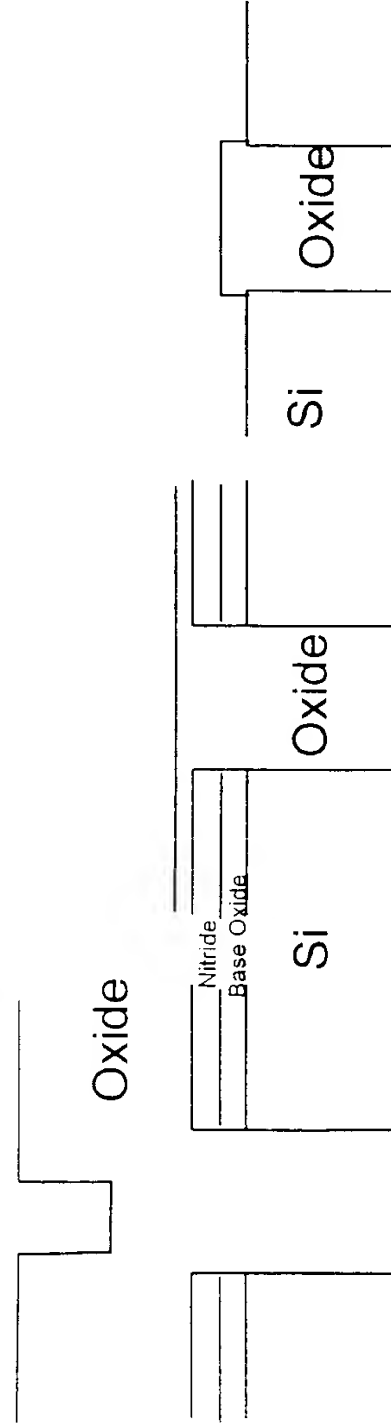
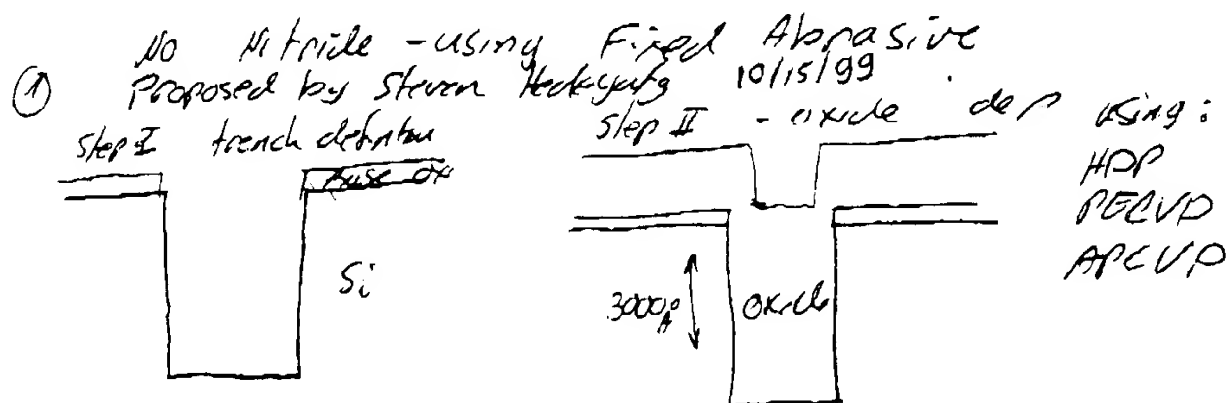


Exhibit A - page 11

STC

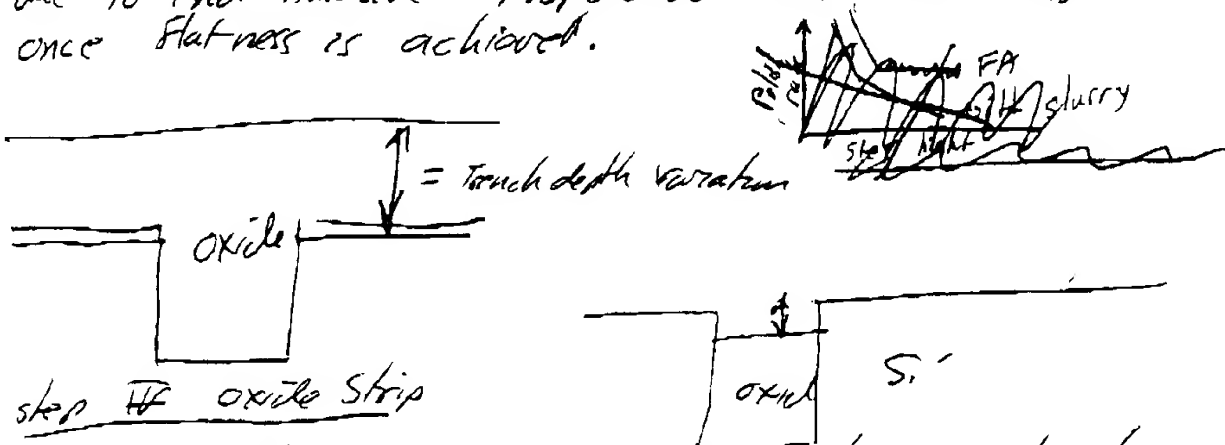
method of making shallow trench isolation
structure with no/or thin nitride CMO step.



in step II
need to deposit trench depth + trench depth variation

step II Polish

due to Fixed Abrasive properties CMP will self planarize
once flatness is achieved.



strip will result in oxide below Si level

Steven Hegedus, Ramkumar, Bill Kothari, Mike Guller

S. Hegedus
H. Blossie

11/15/99

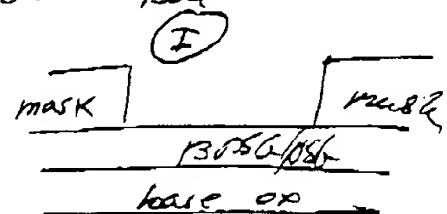
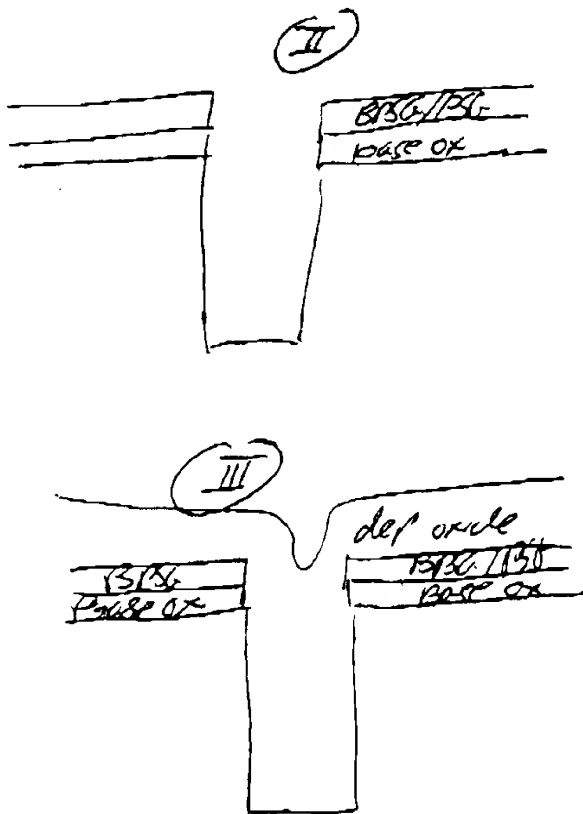
11/15/99

Exhibit B - page 1

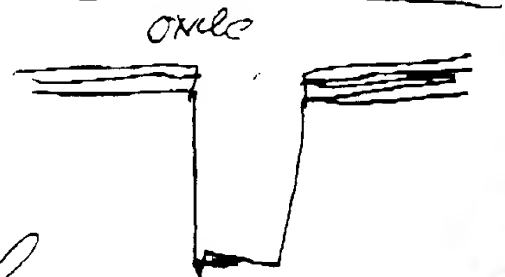
STC

as long as trench depth variation is controlled below a certain number ie $\pm 500 \text{ \AA}$ then polish can be done without ~~the~~ nitride layer.

(2) 2nd method use of PSI/PSG layer as a base oxide or on top of base oxide



(IV) Polish using Fixed Abrasive



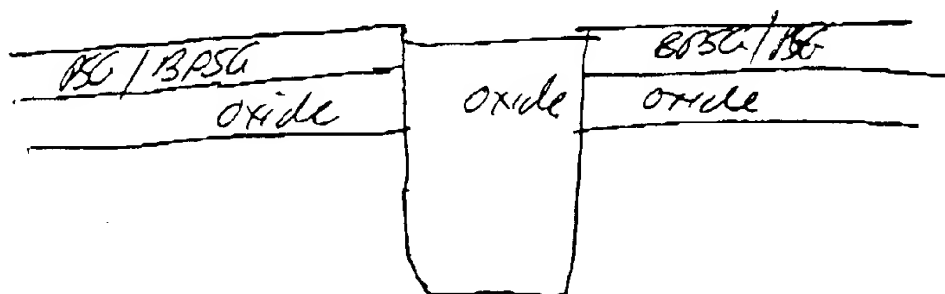
Bll Kouthay B.K. /m
S. Hedgale
Alan Blome

11/15/99
11/15/99

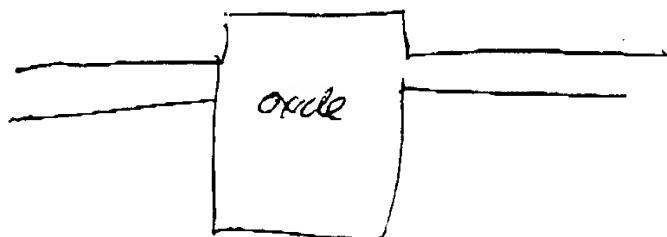
3

~~strip oxide back to BPSG~~

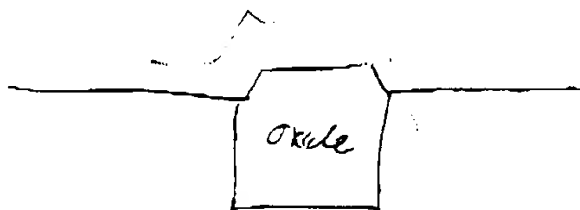
Polish Back to BPSG layer
strip



use wet strip BPSG ER is N 50 times
thermal oxide rate so result will be
after strip I



after strip II



Bill Koutney 1/16/96

J. Hedgcock
DA. 1/17/96

11/15/96
11/15/96

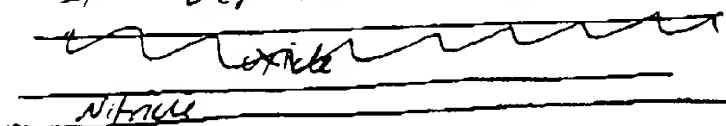
Exhibit B- page 3

Si

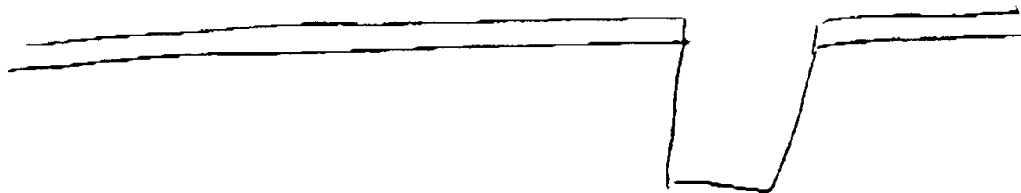
(3) use thin Nitride for Si

Nitride is used only as a means
to determine oxide height above Si

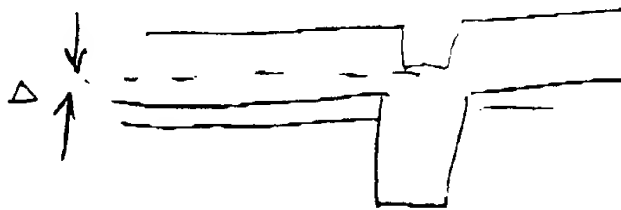
I dep Thin Nitride



II mask and etch



III dep HDP oxide or PECVD oxide or APCVD
oxide



Thickness is
targeted to
achieve planarity
at ΔA above

Si

Bill Kaufman - *Bill*

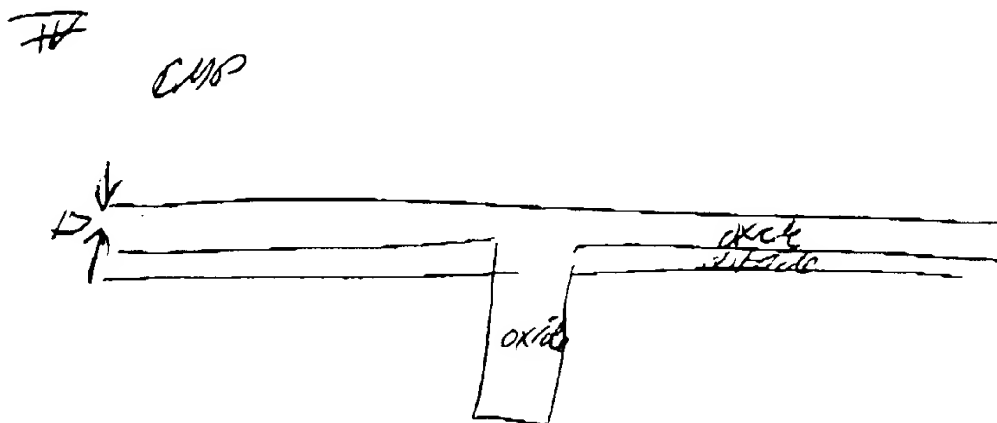
A. Hedger

Alan Blome

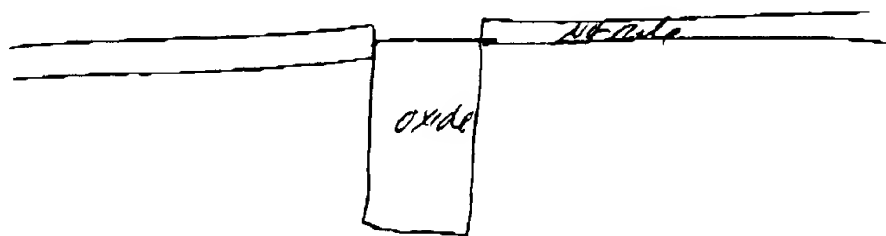
11/15/99

11/15/99

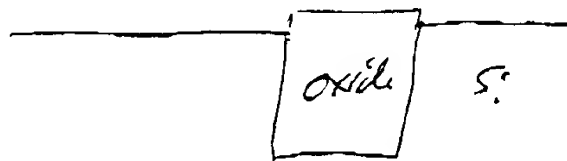
Exhibit B- page 4



V wet strip of oxide



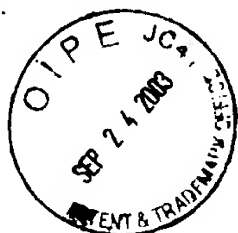
VI nitrate strip



B.1 Kowboy Mike Gilman
S. Hedberg
Flora Blum

11/15/99
11/15/99

Exhibit B - page 5



RECEIVED

SEP 30 2003

TC 1700

PATENT

5298-04700/PM00028

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Gilboa et al.

Serial No.: 09/846,119

Filed: April 30, 2001

For: METHOD OF MAKING A
PLANARIZED SEMICONDUCTOR
STRUCTURE

Group Art Unit: 1763

Examiner: Goudreau, G.

Atty. Dkt. No.: 5298-04700

CERTIFICATE OF MAILING
37 C.F.R. § 1.18

I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on the date indicated below.

9-19-03
Date

Kevin L. Daffer

DECLARATION UNDER 37 C.F.R. § 1.131

Commissioner for Patents
Washington, D.C. 20231

I, Krishnaswamy Ramkumar, hereby declare and state that:

1. I am a named inventor in the above-identified patent application, which is U.S. Patent Application No. 09/846,119, filed on April 30, 2001.
2. I have been informed that in the present application, certain claims have been rejected on reference to an article in *Solid State Technology* entitled Improved Planarization for STI with Fixed Abrasive Technology by Vo et al., which was published in June of 2000.

RECEIVED

SEP 26

OFFICE OF PETITIONS

CONCEPTION

3. As supported below, I, along with Yitzhak Gilboa, William W.C. Koutny, Jr. and Steven Hedayati, conceived of the subject matter claimed in the present application within the United States before June of 2000. The subject matter includes a method for forming a structure within a trench of a semiconductor topography.

4. Exhibit A attached hereto is a true copy of an invention disclosure form and attached pages which bear dates before June of 2000 corresponding to the conception of the invention. The actual dates for the first drawings, the first written description and first oral disclosure to others have been redacted.

5. Page 5 of Exhibit A describes the subject matter of the presently claimed case including the use of fixed abrasive polishing techniques to produce structures with a limited amount of dishing.

6. Exhibit B attached hereto is a true copy of a written description of the conceived subject matter, dated before June of 2000.

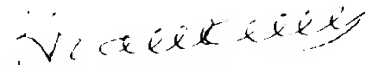
7. Page 2 of Exhibit B describes the subject matter of the rejected claims including the use of fixed abrasive polishing techniques to polish a layer deposited within a trench.

REDUCTION TO PRACTICE AND DILIGENCE

8. From at least a time just prior to June of 2000 through the filing of the application on April 30, 2001, plans were undertaken to prepare the captioned patent application, which was commissioned to Kevin Daffer at Conley, Rose & Tayon, P.C. I did not abandon, suppress, or conceal the ideas set forth in the claimed invention during at least the time beginning just prior to June of 2000 through the filing of the application on April 30, 2001.

9. Upon information and belief, it is my informed understanding that diligence in reducing the invention to practice was therefore maintained from at least as early as just prior to June of 2000 through the filing of the application on April 30, 2001.

10. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.



Krishnaswamy Ramkumar

Date: 1/19/03

CONLEY ROSE, P.C.

INTELLECTUAL PROPERTY LAW
INCLUDING
PATENTS, TRADEMARKS,
COPYRIGHTS AND
UNFAIR COMPETITION

A PROFESSIONAL CORPORATION
THE CHASE BUILDING
700 LAVACA, SUITE 720
AUSTIN, TEXAS 78701-3108
(512) 476-1400
FACSIMILE (512) 703-1250
www.conley-rose.com

HOUSTON OFFICE
CHASE TOWER
600 TRAVIS, SUITE 7100
HOUSTON, TEXAS 77002-2912
(713) 238-8000
FACSIMILE (713) 238-8008

KEVIN L. DAFFER
(512) 476-1400
kdaffer@conley-rose.com

5298-04700

August 21, 2003

Steven Hedayati
1240 Valley Quail Circle
San Jose, CA 95120

Via Certified Mail, RRR

Re: Declaration to Predate Reference with Regard to Cypress Patent Application PM00028

Dear Mr. Hedayati:

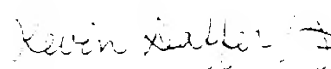
I am contacting you in regard to a patent application filed on behalf of Cypress Semiconductor Corporation. You are listed as a co-inventor of the invention, along with Yitzhak Gilboa, Krishnaswamy Ramkumar and William W. C. Koutny, Jr. The application is entitled "Method of Making a Planarized Semiconductor Substrate" and Cypress's reference number is PM00028. The application was filed on April 30, 2001.

We have received a rejection from the U.S. Patent and Trademark Office citing some patents and publications which teach some of the limitations claimed in the patent application. One of the references may be overcome by filing a declaration that the conception date of the invention is prior to the publication date of the cited reference. Enclosed herein is a copy of such a declaration. Please review, sign and return the enclosed declaration as soon as possible. Your immediate attention to this matter is appreciated.

I have also attached a copy of the invention disclosure form and copies of Yitzhak's lab notebook pertaining to the patent application. The documents will be filed with the declarations as Exhibits A and B, respectively. As noted in the declarations, the reference we are declaring to predate is an article in *Solid State Technology* entitled "Improved Planarization for STI with Fixed Abrasive Technology" by Vo et al., which was published in June of 2000. If you would like me to send you a copy of the article, please let me know.

Please do not hesitate to call me at (512) 703-1242 if you have any questions.

Very truly yours,



Kevin L. Daffer

Enclosure

RECEIVED

SEP 26

OFFICE OF PETITIONS

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

1. INVENTOR(S)

DISCLOSURE NO PM00028

A. Name YITZHAK GILSON CY Initials YEG Empl. No. 73035 Ext. No. 2719
 Citizenship USA Dept # 300 Home Phone No. 408-253-2507
 Home Mailing Address 1761 HERON AVE SCARSDALE, NY 11767

B. Name William Binstrey CY Initials BK Empl. No. 135 Ext. No. 263
 Citizenship US Dept # Home Phone No. 408-247-0505
 Home Mailing Address 7335 Highway #45 Santa Clara, CA 95051
2729 Homestead 45 95051

C. Name Steven Hedgati CY Initials SSH Empl. No. 8534 Ext. No. 4556
 Citizenship US Dept # 3108 Home Phone No. 408-927-0187
 Home Mailing Address 1240 Valley Quail Circle San Jose, CA 95120

2. TITLE OF INVENTION Method of making Shallow trench isolation structure

3. CONCEPTION OF INVENTION

A. Date of first drawing or drawings Redacted
 Where can first drawing be found Redacted
 B. Date of first written description Redacted
 Where is description found Redacted
 C. Date of first oral disclosure to others Redacted
 To whom? discussed with KTR, SSH, BK

4. CONSTRUCTION OF DEVICE

A. Date Completed
 B. Was prototype made?
 C. By whom made?
 D. Where can the prototype be found?

Inventors: William Binstrey Date 11/21/90
 Inventors: Steven Hedgati Date 5/24/90
 Inventors: Yitzhak Gilson Date 8/20/90
 Witnessed, Read, and Understood by: [Signature] Date 8/20/90
 Witnessed, Read, and Understood by: [Signature] Date 8/20/90

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

1. INVENTOR(S)

DISCLOSURE NO. _____

A. Name Ramkumar CY Initials KTR Empl. No. 3305 Ext. No. 2720
Citizenship INDIAN Dept # 3108 Home Phone No. (408) 255-1031
Home Mailing Address 1193 LYNBROOK WAY, SAN JOSE, CA 95128

B. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____
Citizenship _____ Dept # _____ Home Phone No. _____
Home Mailing Address _____

C. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____
Citizenship _____ Dept # _____ Home Phone No. _____
Home Mailing Address _____

2. TITLE OF INVENTION _____

3. CONCEPTION OF INVENTION

- A. Date of first drawing or drawings _____
Where can first drawing be found _____
- B. Date of first written description _____
Where is description found _____
- C. Date of first oral disclosure to others _____
To whom? _____

4. CONSTRUCTION OF DEVICE

- A. Date Completed _____
- B. Was prototype made? _____
- C. By whom made? _____
- D. Where can the prototype be found? _____

Inventor(s): _____ Date _____

Inventor(s): _____ Date _____

Inventor(s): _____ Date _____

Witnessed, Read and Understood by _____ Date _____

Witnessed, Read and Understood by _____ Date _____

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CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

5. TEST OF DEVICE

A. Date: Witness(es): B. Results:

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A. Was invention sold or offered for sale? Yes No ✓B. Was invention used to make, assemble or test a commercial product? Yes No ✓C. Will invention be sold, offered for sale, sampled, or used to make, assemble or test a commercial product? Yes No ✓D. Actual or estimated date of first sale, offer or commercial use E. Is invention part of a product for which there is a data sheet? Yes No ✓ (If yes, attach a copy)F. Actual or estimated date of publication, release or availability of data sheet

7. USE

A. Is invention presently being used? Yes No ✓B. In what product or process is invention presently being used?

 Are there specific plans for its use in near future? In what products or processes?
RAM-D

8. RELATED PRINTED PUBLICATIONS, PATENTS, PATENT APPLICATIONS

5,972,792 / 4,010,523 and 5,782,675 / 5,919,072
4,396,271 - RAM - D9. WAS INVENTION Conceived (Yes (No ✓ Constructed (Yes (No ✓ Tested (Yes (No ✓ during performance of Government Contract?Contract Number
(Give Full Contract Number)

The description of invention should be written in the inventor's own words and generally should follow the outline given below. Sketches, prints, photos, and other illustrations, as well as memos or reports of any

Inventor(s): <u> </u>	Date: <u> </u>
Inventor(s): <u> </u>	Date: <u> </u>
Inventor(s): <u> </u>	Date: <u> </u>
Witnessed, Read, and Understood by: <u> </u>	Date: <u> </u>
Witnessed, Read, and Understood by: <u> </u>	Date: <u> </u>

Each page upon which information is entered should be signed and witnessed.

Exhibit A - page 3

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

FOR ANSWERS TO THE FOLLOWING QUESTIONS, USE THE REMAINDER OF SHEET AND THE ATTACHED SHEET(S).

1. General purpose of invention. State in general terms the objects of the invention.
2. Describe old technology, if any, for performing the function of the invention. Provide references, if available.
3. Indicate the disadvantages of the old technology.
4. Describe your invention and its construction, showing the changes, additions and improvements over the old method.
5. Give details of its operation (i.e., how is your invention used?), if not already described under 4.
6. State the advantages of your invention over what has been done before.
7. Indicate any alternate component(s) and/or method(s) of construction.
8. If a joint invention, indicate what contribution was made by each inventor.
9. Describe the features that are believed to be new.
10. State opinion of relative value of invention.
- ***
11. After the disclosure is prepared, it should be signed by the inventor(s) and then read and signed by two witnesses in the space provided at the bottom of each sheet. Forward an electronic copy of this form, as well as a paper copy bearing original signatures, to the Intellectual Property Department.

=====

1. The purpose of the invention is to improve the manufacturability of STI and reduce cost, by a more reducing processing steps.

2. Current technology (ST-40 TOR) calls for the following steps:

1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13. 14. 15. 16. 17. 18. 19. 20. 21. 22. 23. 24. 25. 26. 27. 28. 29. 30. 31. 32. 33. 34. 35. 36. 37. 38. 39. 40. 41. 42. 43. 44. 45. 46. 47. 48. 49. 50. 51. 52. 53. 54. 55. 56. 57. 58. 59. 60. 61. 62. 63. 64. 65. 66. 67. 68. 69. 70. 71. 72. 73. 74. 75. 76. 77. 78. 79. 80. 81. 82. 83. 84. 85. 86. 87. 88. 89. 90. 91. 92. 93. 94. 95. 96. 97. 98. 99. 100.

| | | | |
|-------------------------------------|----------------------|-------|----------------|
| Inventor(s): | <u>Wahid Murtuza</u> | Date: | <u>8/24/00</u> |
| Inventor(s): | <u>S. Sadiq</u> | Date: | <u>8/24/00</u> |
| Inventor(s): | <u>[Signature]</u> | Date: | <u>8/24/00</u> |
| Witnessed, Read, and Understood by: | <u>[Signature]</u> | Date: | <u>8/24/00</u> |
| Witnessed, Read, and Understood by: | <u>S. Sadiq</u> | Date: | <u>8/24/00</u> |

Each page upon which information is entered should be signed and witnessed.

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

nature in which the invention is referred to, if available, should form a part of this disclosure and reference can be made thereto in the descriptions of the invention's construction and operation.

3. Disadvantages addressed by invention:

1. Trade nitride - layer required to overcome self etching in etching case
2. Process - this means can include stress effects
3. Additional etch required to etch nitride
4. Small step after nitride strip which can result in self etching
5. Further oxide film deposition to overcome step induced by nitride

4. The current invention has three options all using Fixed Abrasive polish as the ~~main~~ method of polish. The main advantage of Fixed Abrasive is the negligible amount of dishing compared to conventional etching processes. The second advantage is self alignment. Both are requirements of the option I - no nitride hard mask.

In this option no nitride is used. Etching is done on base oxide trench and range is of one step or more. The trench is opened, after trench etch oxide film is grown in the trench and across the surface a thickness of the trench + trench depth variation. After oxide deposition the oxide is polished using Fixed Abrasive to a nominal thickness of 0-500 Å. The last step requires a self alignment step to ensure the etch mask is self aligned to the trench.

| | | | |
|-------------------------------------|-------------------------|-------|-----------------|
| Inventor(s): | <u>William M. Smith</u> | Date: | <u>11/20/80</u> |
| Inventor(s): | <u>J. H. Smith</u> | Date: | <u>11/20/80</u> |
| Inventor(s): | <u>[Signature]</u> | Date: | <u>11/20/80</u> |
| Witnessed, Read, and Understood by: | <u>[Signature]</u> | Date: | <u>11/20/80</u> |
| Witnessed, Read, and Understood by: | <u>[Signature]</u> | Date: | <u>11/20/80</u> |

Each page upon which information is entered should be signed and witnessed.

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

Option II - Deposit Thin Nitride -

grow base oxide grow thin layer of Nitride (5-500Å)
 expose field oxide mask, Etch trench, Deposit fill oxide
 polish down to ~~1000~~ stop on oxide at a predetermined
 residual oxide where the nitride. Strip remaining oxide.
 Stop remaining nitride.

Option III

grow base oxide deposit PPSG/PSG, expose trench
 Etch trench, deposit fill oxide. Etch to PPSG/PSG layer
 use wet strip to remove remaining PPSG, use buffered
 wet strip to remove oxide, then a wet Etch Rate
 difference of oxide to remove oxide and then
 polish to remove stop of Nitride only leave 50.

⑥ - To be aware of patent preparation of this invention
 showing the use of this as a patentable idea.

⑦ - This is a very basic idea for a patent covering a
 new process for growing a gate oxide layer.

| | | | |
|-------------------------------------|-------------------------|-------|----------------|
| Inventor(s): | <u>William M. Smith</u> | Date: | <u>5/20/77</u> |
| Inventor(s): | <u>J. Hedger</u> | Date: | <u>5/20/77</u> |
| Inventor(s): | <u>John J. Smith</u> | Date: | <u>5/20/77</u> |
| Witnessed, Read, and Understood by: | <u>[Signature]</u> | Date: | <u>5/20/77</u> |
| Witnessed, Read, and Understood by: | <u>[Signature]</u> | Date: | <u>5/20/77</u> |

Each page upon which information is entered should be signed and witnessed.

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

- (8) equal contribution
- (9) Fixed abrasive polish, no polish step, different Polish steps
- (10) - Invention will enable reduction of cost of ownership compared to Slurry.
 - enables STC polish without requirement of Reverse wash.
 - enables STC polish with reduced step in the budget required for its own lithography.

```
inventor(s;
```

Wm. H. Hunt

Date _____

6-2-2

invertorisi;

5. 1000

2. वाप

5/24/20

over:0715;

6044

Date _____

2257

Witnessed, Read and Understood by:

Read and Understood by:

Life

7-5-100

Witnessed Read and Understood by

Read and Understood by: El S. J. 26

Date _____

2/2/42

Each page upon which information is entered should be signed and witnessed.



CYPRESS

STI Invention Disclosure

Option 1

- No Nitride IIM
- Stop after flatness - fixed abrasive
- Wet dip to below Si

CMP

HF dip

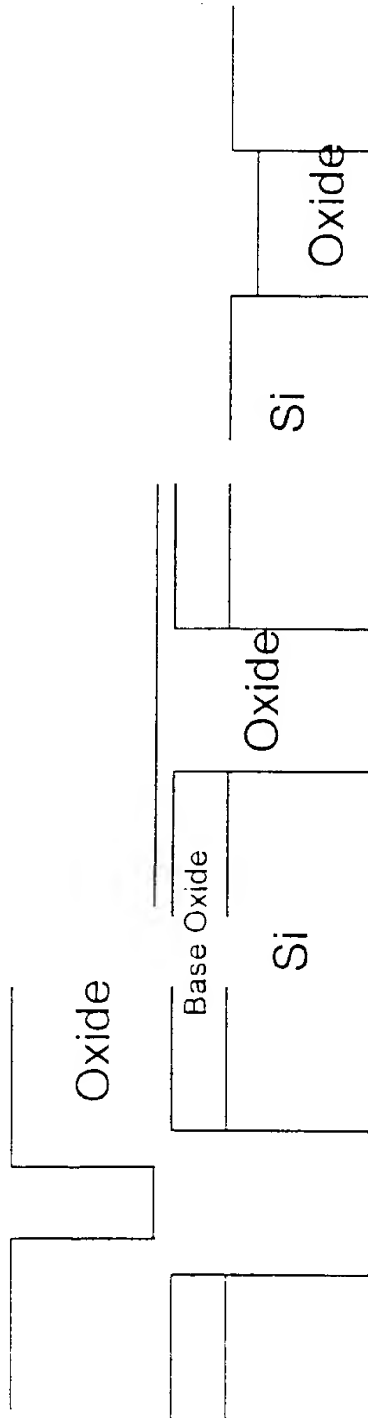


Exhibit A- page 8



CYPRESS

STI Invention Disclosure

Method of Making STI

Option 1

WD4 #03

24-AUG-00
dense

Depth 43nm

10.0kV X80.0k 375nm

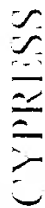
WD5 #01

25-AUG-00

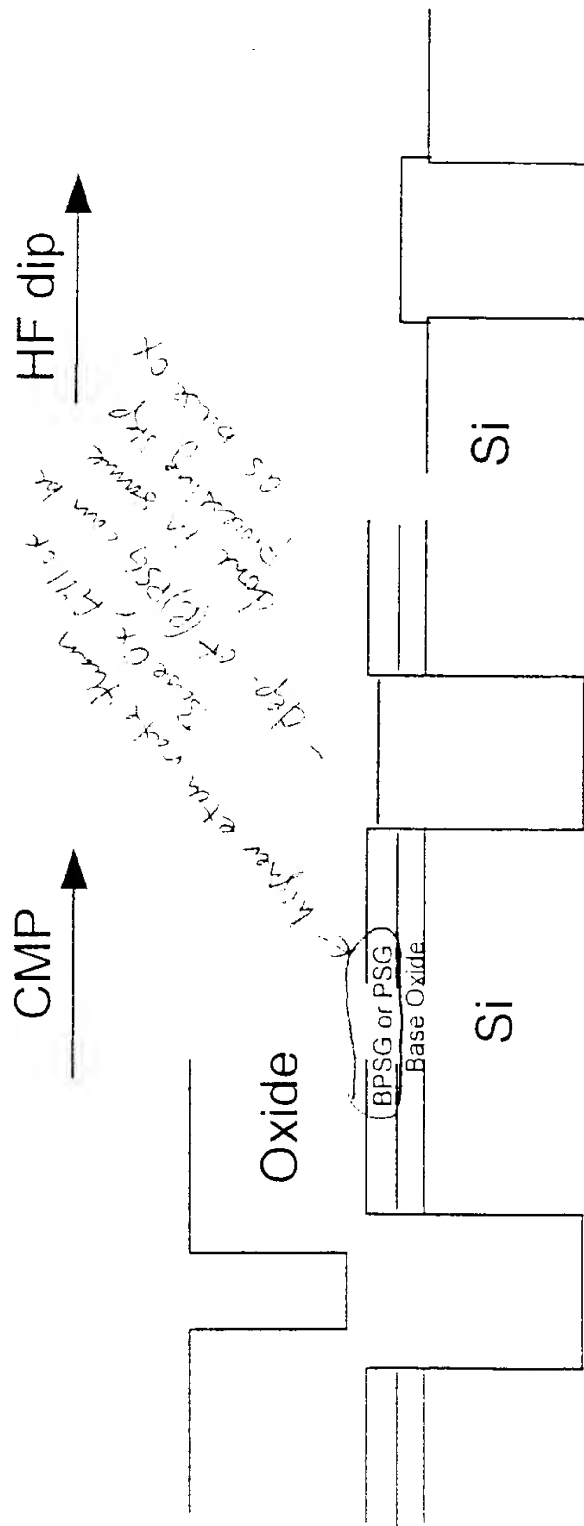
**X : 0.000nm
**D : 320.0nm

10.0kV X80.0k 375nm

Exhibit A- page 9



- Use doped oxide to increase selectivity during wet Dip
- polish to flatness - Fixed Abrasive
- Wet dip - ratio of doped oxide thickness to un-doped thickness controls step height





CYPRESS

STI Invention Disclosure

Option 3

→ Nitride Nitride (Nitride) to
etch as CMP polish stop

- Use thin Nitride
- polish to flatness - Fixed Abrasive, stop with oxide over Nitride, nitride is used to determine the step height and not as polish stop.
- Wet dip - Nitride thickness controls step height

CMP

HF dip + Nitride Strip

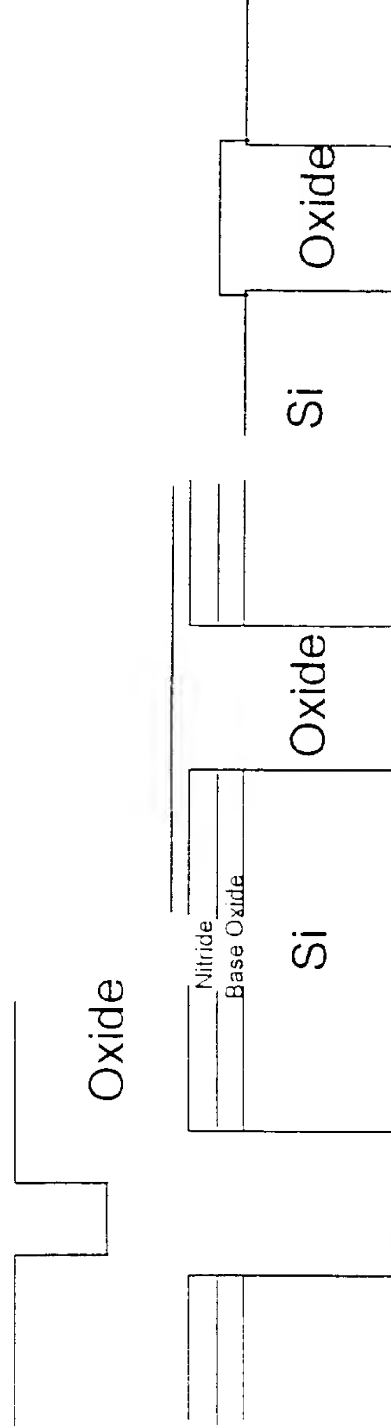
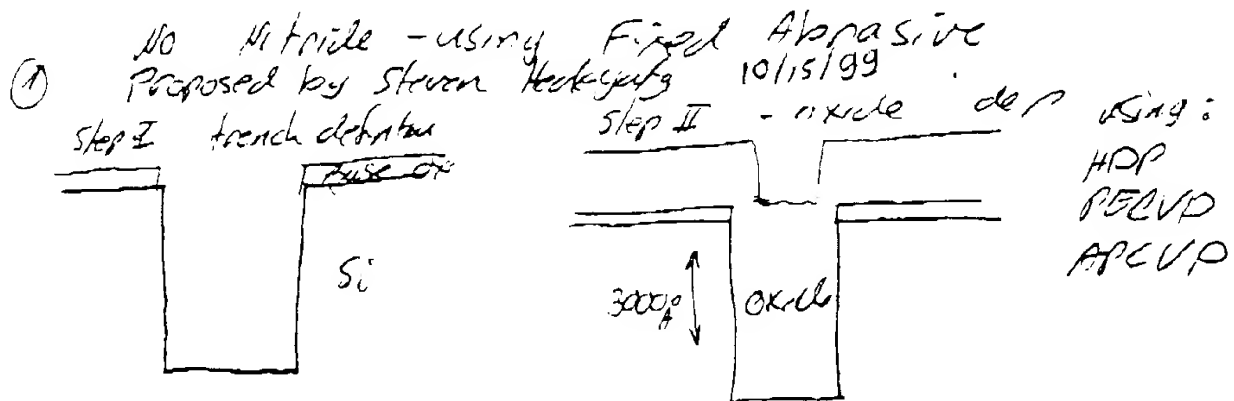


Exhibit A - page 11

STC

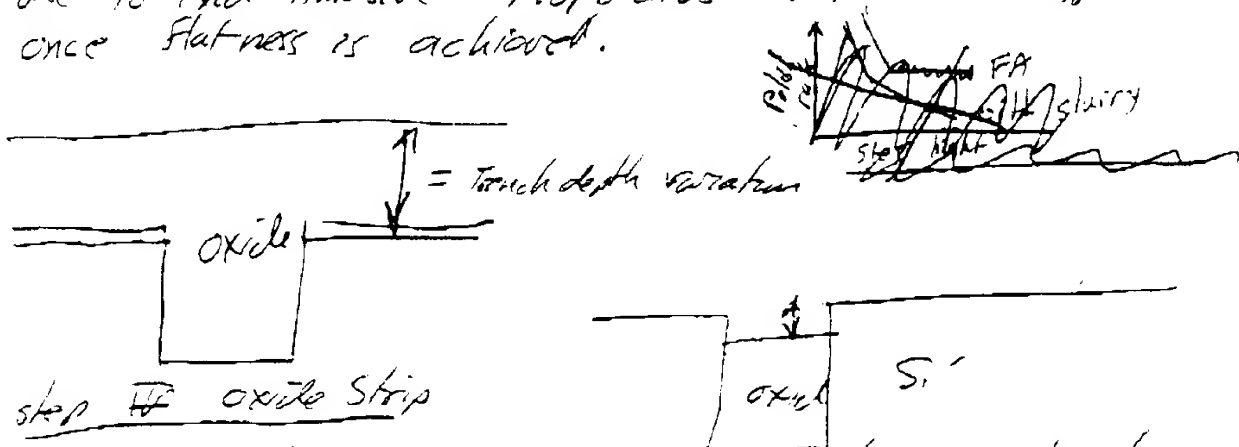
method of making shallow trench isolation
structure with no/or thin nitride CMO stop.



in step II
need to deposit trench depth + trench depth variation

step II polish

due to Fixed Abrasive properties CMP will self planarize
once flatness is achieved.



strip will result in oxide below Si level

Steven Hegarty, Ramkumar, Bill Katay, Mike Allison

S. Hegarty
H. Blom

11/15/99

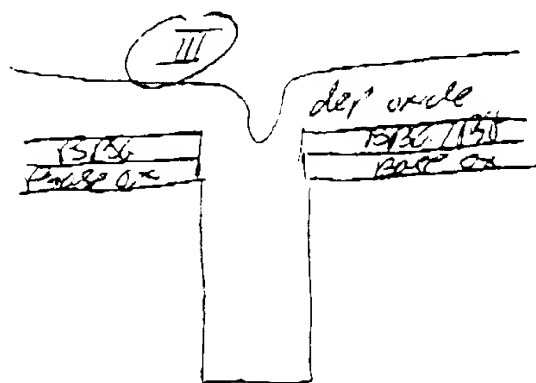
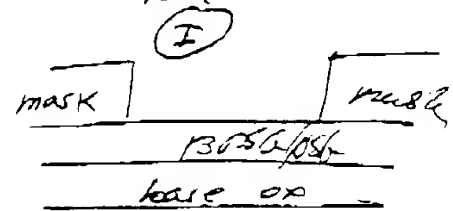
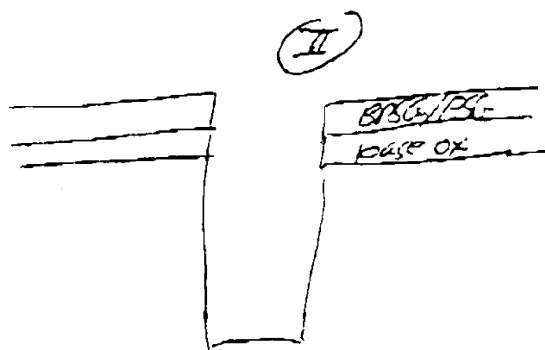
11/15/99

Exhibit B - page 1

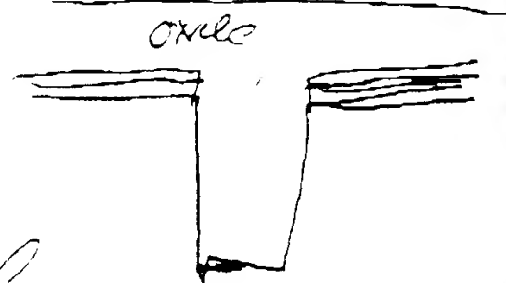
577

as long as trench depth variation is controlled below a certain number ie ± 500 Å then polish can be done without ~~the~~ nitride layer.

② 2nd method use of ps/BPSG layer as a base oxide or on top of base oxide



Polish using Final Abrasive



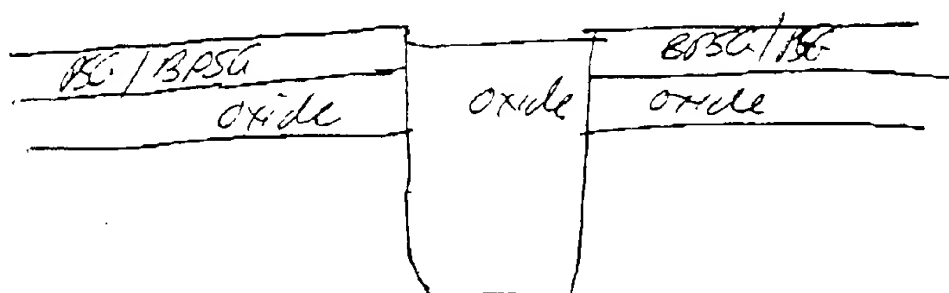
Bill Koutney R.K. M
S. Hedgeli
Alan Blore

11/15/89
11/15/89

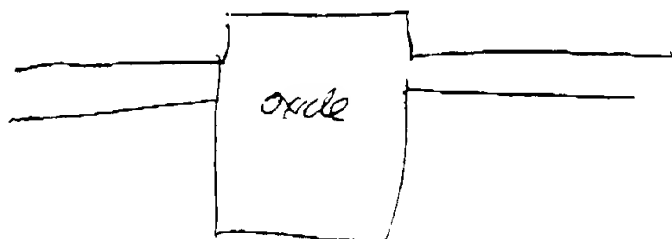
3

~~strip oxide back to BPSG~~

Polish Back to BPSG layer
strip



use wet strip BPSG ER is ~50 times
thermal oxide rate so result will be
after strip I



after strip II



Bill Koutinos / Mike Collier
J. Hedgcock
D.H. / D.H.

11/15/99
11/15/99

Exhibit B - page 3

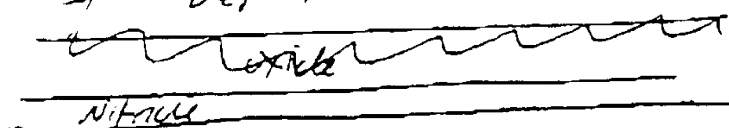
Si

(3)

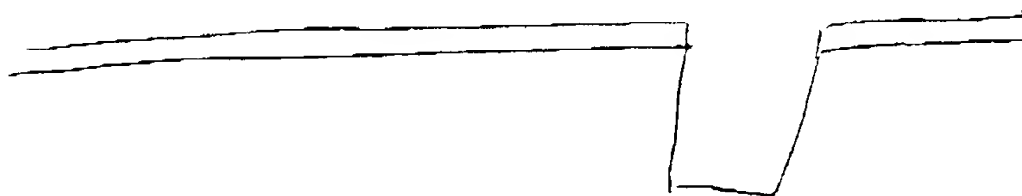
use thin Nitride for Si

Nitride is used only as a means
to determine oxide height above Si

I. dep thin Nitride

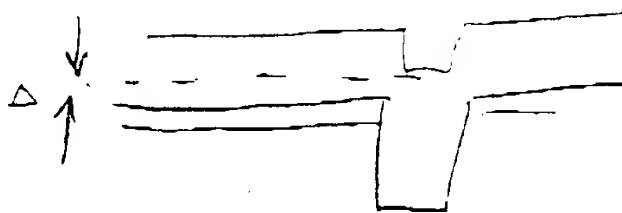


II. mask and etch



III

dep HDP oxide or PECVD oxide or APCVD
oxide



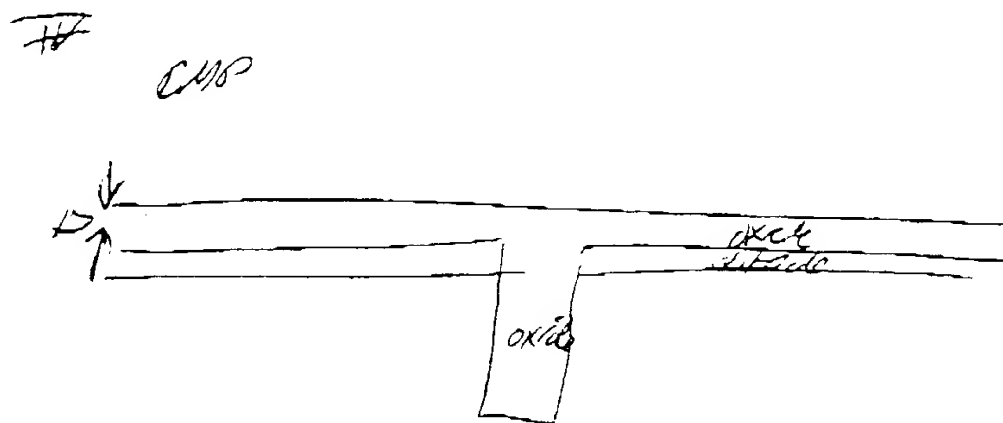
Thickness is
targeted to
achieve planarity
at DA above

Si

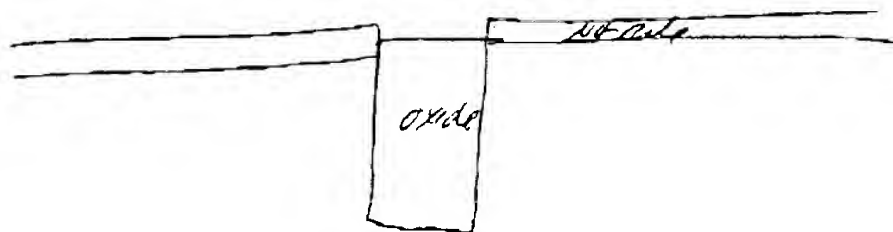
Bill Kautz - 12/1/99
S. Hedger
Alan Blose

11/15/99 -
11/15/99 -

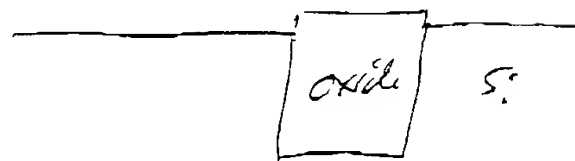
Exhibit B- page 4



IV wet strip of oxide



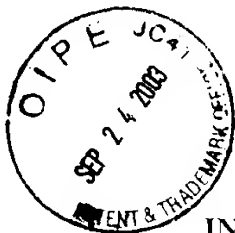
V pure strip



Bill Kennedy White Galloway
 S. Hedgcock
 Alani Blum

10/15/99
 10/15/99

Exhibit B - page 5



PATENT
5298-04700/PM00028

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Gilboa et al.

Serial No.: 09/846,119

Filed: April 30, 2001

For: METHOD OF MAKING A
PLANARIZED SEMICONDUCTOR
STRUCTURE

Group Art Unit: 1763

Examiner: Goudreau, G.

Atty. Dkt. No.: 5298-04700

CERTIFICATE OF MAILING
37 C.F.R. § 1.18

I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on the date indicated below.

9-19-03
Date

Kevin L. Daffer

DECLARATION UNDER 37 C.F.R. § 1.131

Commissioner for Patents
Washington, D.C. 20231

I, Yitzhak Gilboa, hereby declare and state that:

1. I am a named inventor in the above-identified patent application, which is U.S. Patent Application No. 09/846,119, filed on April 30, 2001.
2. I have been informed that in the present application, certain claims have been rejected on reference to an article in *Solid State Technology* entitled Improved Planarization for STI with Fixed Abrasive Technology by Vo et al., which was published in June of 2000.

CONCEPTION

3. As supported below, I, along with Steven Hedayati, William W.C. Koutny, Jr. and Krishnaswamy Ramkumar, conceived of the subject matter claimed in the present application within the United States before June of 2000. The subject matter includes a method for forming a structure within a trench of a semiconductor topography.

4. Exhibit A attached hereto is a true copy of an invention disclosure form and attached pages which bear dates before June of 2000 corresponding to the conception of the invention. The actual dates for the first drawings, the first written description and first oral disclosure to others have been redacted.

5. Page 5 of Exhibit A describes the subject matter of the presently claimed case including the use of fixed abrasive polishing techniques to produce structures with a limited amount of dishing.

6. Exhibit B attached hereto is a true copy of a written description of the conceived subject matter, dated before June of 2000.

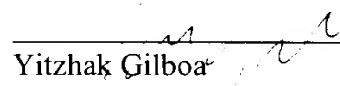
7. Page 2 of Exhibit B describes the subject matter of the rejected claims including the use of fixed abrasive polishing techniques to polish a layer deposited within a trench.

REDUCTION TO PRACTICE AND DILIGENCE

8. From at least a time just prior to June of 2000 through the filing of the application on April 30, 2001, plans were undertaken to prepare the captioned patent application, which was commissioned to Kevin Daffer at Conley, Rose & Tayon, P.C. I did not abandon, suppress, or conceal the ideas set forth in the claimed invention during at least the time beginning just prior to June of 2000 through the filing of the application on April 30, 2001.

9. Upon information and belief, it is my informed understanding that diligence in reducing the invention to practice was therefore maintained from at least as early as just prior to June of 2000 through the filing of the application on April 30, 2001.

10. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.


Yitzhak Gilboa

Date:

7/14/03

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

1. INVENTOR(S)

DISCLOSURE NO PM00028

A. Name YITZHAK GURON CY Initials YEG Empl. No. 7335 Ext. No. 7719
 Citizenship USA Dept # 308 Home Phone No. 408-253-3507
 Home Mailing Address 1761 HERMAN AVE SCARSDALE, NY 11757

B. Name William Kinney CY Initials BK Empl. No. 135 Ext. No. 363
 Citizenship US Dept # Home Phone No. 408-247-0555
 Home Mailing Address 755 Homestead #45 Santa Clara, CA 95051
2555 Homestead 45 95051

C. Name Steven Hedvick CY Initials SH Empl. No. 3534 Ext. No. 4556
 Citizenship US Dept # 3103 Home Phone No. 408-927-9187
 Home Mailing Address 1240 Valley Quail Circle San Jose, CA 95120

2. TITLE OF INVENTION Method of making Si/SiO₂ trench isolation structure

3. CONCEPTION OF INVENTION

A. Date of first drawing or drawings Redacted
 Where can first drawing be found Redacted
 B. Date of first written description Redacted
 Where is description found Redacted
 C. Date of first oral disclosure to others Redacted
 To whom? discussed with KTR, SJE, BIK

4. CONSTRUCTION OF DEVICE

A. Date Completed
 B. Was prototype made?
 C. By whom made?
 D. Where can the prototype be found?

| | |
|--|----------------------|
| Inventor(s): <u>William Kinney</u> | Date: <u>1/24/88</u> |
| Inventor(s): <u>S. Hedvick</u> | Date: <u>5/24/88</u> |
| Inventor(s): <u>Y. Guron</u> | Date: <u>8/24/88</u> |
| Witnessed, Read, and Understood by: <u>[Signature]</u> | Date: <u>8/24/88</u> |
| Witnessed, Read, and Understood by: <u>[Signature]</u> | Date: <u>8/24/88</u> |

Each page upon which information is entered should be signed and witnessed.

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

1. INVENTOR(S)

DISCLOSURE NO. _____

A. Name Banburat CY Initials KTB Empl. No. 3305 Ext. No. 2720
Citizenship INDIAN Dept # 3108 Home Phone No. (408) 255-1031
Home Mailing Address 1193 LYNBROOK WAY, SAN JOSE, CA 95128

B. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____
Citizenship _____ Dept # _____ Home Phone No. _____
Home Mailing Address _____

C. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____
Citizenship _____ Dept # _____ Home Phone No. _____
Home Mailing Address _____

2. TITLE OF INVENTION _____

3. CONCEPTION OF INVENTION

- A. Date of first drawing or drawings _____
Where can first drawing be found _____
- B. Date of first written description _____
Where is description found _____
- C. Date of first oral disclosure to others _____
To whom? _____

4. CONSTRUCTION OF DEVICE

- A. Date Completed _____
- B. Was prototype made? _____
- C. By whom made? _____
- D. Where can the prototype be found? _____

Inventor(s): _____ Date _____

Inventor(s): _____ Date _____

Inventor(s): _____ Date _____

Witnessed, Read, and Understood by: _____ Date _____

Witnessed, Read, and Understood by: _____ Date _____

Each page upon which information is entered should be signed and witnessed

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

5. TEST OF DEVICE

A. Date: _____ Witness(es): _____

B. Results: _____

6. SALE

A. Was invention sold or offered for sale? Yes ☐ No ☒

B. Was invention used to make, assemble or test a commercial product? Yes ☐ No ☒

C. Will invention be sold, offered for sale, sampled, or used to make, assemble or test a commercial product? Yes ☐ No ☒

D. Actual or estimated date of first sale, offer or commercial use _____

E. Is invention part of a product for which there is a data sheet? Yes ☐ No ☒ (If yes, attach a copy)

F. Actual or estimated date of publication, release or availability of data sheet _____

7. USE

A. Is invention presently being used? Yes _____ No ✓

B. In what product or process is invention presently being used?

Are there specific plans for its use in near future? In what products or processes?

RAM-P

8. RELATED PRINTED PUBLICATIONS, PATENTS, PATENT APPLICATIONS

5,972,792 / 4010583 / 5782675 / 5919082

9. **WAS INVENTION** Conceived (Yes ☐ (No ☒ Constructed (Yes ☐ (No ☒ Tested (Yes ☐ (No ☒ during performance of Government Contract?

Contract Number _____
(Give Full Contract Number)

The description of invention should be written in the inventor's own words and generally should follow the outline given below. Sketches, prints, photos, and other illustrations, as well as memos or reports of any

Inventor(s) Walter Smith Date 5/27/00

Inventor's: A. H. Hirsch Date 6/20/00

Inventory: _____ Date: 02/24/0

Witnessed, Read, and Understood by: [Signature] Date: 8/20/04

Witnessed, Read, and Understood by U. S. [Signature] Date 8/24/00

Document No. 27-00000 Rev. 'D

Page 2 of 3

Exhibit A - page 3

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

FOR ANSWERS TO THE FOLLOWING QUESTIONS, USE THE REMAINDER OF SHEET AND THE ATTACHED SHEET(S).

1. General purpose of invention. State in general terms the objects of the invention.
2. Describe old technology, if any, for performing the function of the invention. Provide references, if available.
3. Indicate the disadvantages of the old technology.
4. Describe your invention and its construction, showing the changes, additions and improvements over the old method.
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7. Indicate any alternate component(s) and/or method(s) of construction.
8. If a joint invention, indicate what contribution was made by each inventor.
9. Describe the features that are believed to be new.
10. State opinion of relative value of invention.
- ***
11. After the disclosure is prepared, it should be signed by the inventor(s) and then read and signed by two witnesses in the space provided at the bottom of each sheet. Forward an electronic copy of this form, as well as a paper copy bearing original signatures, to the Intellectual Property Department.

=====

1. The purpose of the invention is to improve the manufacturability of STI and reduce cost, this is done by reducing processing steps

2. Current technology (BT-12 TOR) calls for the following steps:

1212 → 1212.1 → 1212.2 → 1212.3 → 1212.4 → 1212.5 → 1212.6 → 1212.7 → 1212.8 → 1212.9 → 1212.10 → 1212.11 → 1212.12 → 1212.13 → 1212.14 → 1212.15 → 1212.16 → 1212.17 → 1212.18 → 1212.19 → 1212.20 → 1212.21 → 1212.22 → 1212.23 → 1212.24 → 1212.25 → 1212.26 → 1212.27 → 1212.28 → 1212.29 → 1212.30 → 1212.31 → 1212.32 → 1212.33 → 1212.34 → 1212.35 → 1212.36 → 1212.37 → 1212.38 → 1212.39 → 1212.40 → 1212.41 → 1212.42 → 1212.43 → 1212.44 → 1212.45 → 1212.46 → 1212.47 → 1212.48 → 1212.49 → 1212.50 → 1212.51 → 1212.52 → 1212.53 → 1212.54 → 1212.55 → 1212.56 → 1212.57 → 1212.58 → 1212.59 → 1212.60 → 1212.61 → 1212.62 → 1212.63 → 1212.64 → 1212.65 → 1212.66 → 1212.67 → 1212.68 → 1212.69 → 1212.70 → 1212.71 → 1212.72 → 1212.73 → 1212.74 → 1212.75 → 1212.76 → 1212.77 → 1212.78 → 1212.79 → 1212.80 → 1212.81 → 1212.82 → 1212.83 → 1212.84 → 1212.85 → 1212.86 → 1212.87 → 1212.88 → 1212.89 → 1212.90 → 1212.91 → 1212.92 → 1212.93 → 1212.94 → 1212.95 → 1212.96 → 1212.97 → 1212.98 → 1212.99 → 1212.100

Inventors: William M. Smith Date: 8/24/00

Inventors: J. H. Smith Date: 8/24/00

Inventors: W. H. Smith Date: 8/24/00

Witnessed, Read, and Understood by: W. H. Smith Date: 8/24/00

Witnessed, Read, and Understood by: W. H. Smith Date: 8/24/00

Each page upon which information is entered should be signed and witnessed

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

nature in which the invention is referred to, if available, should form a part of this disclosure and reference can be made thereto in the descriptions of the invention's construction and operation.

3. Disadvantages addressed by invention:

1. Trade nitride - layer required to overcome surface etching in etching steps
2. Process this nitride can include stress defects.
3. Additional etch required to etch nitride
4. Etch step after nitride etch which can result in poly stringing
5. Further etch for deposition to overcome steps induced by nitride.

4. The current invention has three options in using

Fixed Abrasive paper as the ~~main~~ method of polish.

The main advantage of Fixed Abrasive is the negligible amount of etching compared to conventional etching processes.

The second advantage is self-abrangement. Both rate reducers at the

option I - no nitride layer mask.
In this option no nitride is used. Fixed abrasive on base etch trench etch compared to one step in which the trench is opened. After trench open nitride is deposited in the trench and across the surface a thickness of the nitride + trench depth variation. After etch deposition the case is polished using Fixed Abrasive. A residual thickness of 0-500 Å. The last step compares to a self-abrangement step to remove the seed layer to 0.5 microns or less.

| | | | |
|-------------------------------------|-----------------------|-------|----------------|
| Inventor(s): | <u>James M. Smith</u> | Date: | <u>3/26/88</u> |
| Inventor(s): | <u>J. Smith</u> | Date: | <u>3/26/88</u> |
| Inventor(s): | <u>J. Smith</u> | Date: | <u>3/26/88</u> |
| Witnessed, Read, and Understood by: | <u>[Signature]</u> | Date: | <u>3/26/88</u> |
| Witnessed, Read, and Understood by: | <u>[Signature]</u> | Date: | <u>3/26/88</u> |

Each page upon which information is entered should be signed and witnessed

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

Option II - Deposit Thin Nitride -

grow base oxide grow thin layer of Nitride (0-500Å)
 expose field oxide mask, Etch trench, Deposit fill oxide
 polish down to ~~nitride~~ stop on oxide at a predetermined
 residual oxide above the nitride. Strip remaining oxide.
 Stop Remaining nitride.

Option III

grow base oxide deposit EPSC/PSC, expose field
 Etch trench, deposit fill oxide, polish to EPSC/PSC layer
 use wet strip to remove remaining PSC, use debilitant
 wet strip to remove oxide, then to wet-etch field
 structures of oxide to remove oxide under the field
 polysilicon to remove stop of substrate oxide. Anneal 50.

⑥ - To the knowledge of inventor, properties of - are essential
 to the use of this invention in the field.

⑦ - The inventor is aware that any device or process which requires growing a
 thin oxide stop layer is a patentable invention.

Inventor(s):

William M. Smith

Date

8/20/80

Inventor(s):

J. Hedgcock

Date

8/24/80

Inventor(s):

[Signature]

Date

8/24/80

Witnessed, Read, and Understood by:

[Signature]

Date

8/24/80

Witnessed, Read, and Understood by:

[Signature]

Date

8/24/80

Each page upon which information is entered should be signed and witnessed.

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

- ⑧ equal contact area
- ⑨ Fixed Abrasive polish, no polish step, Different Polish steps
- ⑩ - Inventor will enable reduction of cost of ownership compared to Slury.
 - enable 570 polish without requirement of Reverse polish.
 - enable 570 polish with reduced step in ink budget required for 43 nm technology.

| | |
|--|----------------------|
| Inventor(s): <u>Michael J. McLean</u> | Date: <u>8-28-00</u> |
| Inventor(s): <u>J. McLean</u> | Date: <u>8/28/00</u> |
| Inventor(s): <u>C. J. McLean</u> | Date: <u>8/28/00</u> |
| Witnessed, Read, and Understood by: <u>[Signature]</u> | Date: <u>8-28-00</u> |
| Witnessed, Read, and Understood by: <u>[Signature]</u> | Date: <u>8/28/00</u> |

Each page upon which information is entered should be signed and witnessed.



CYPRESS

Option 1

- No Nitride I/M
- Stop after flatness - fixed abrasive
- Wet dip to below Si

CMP

HF dip

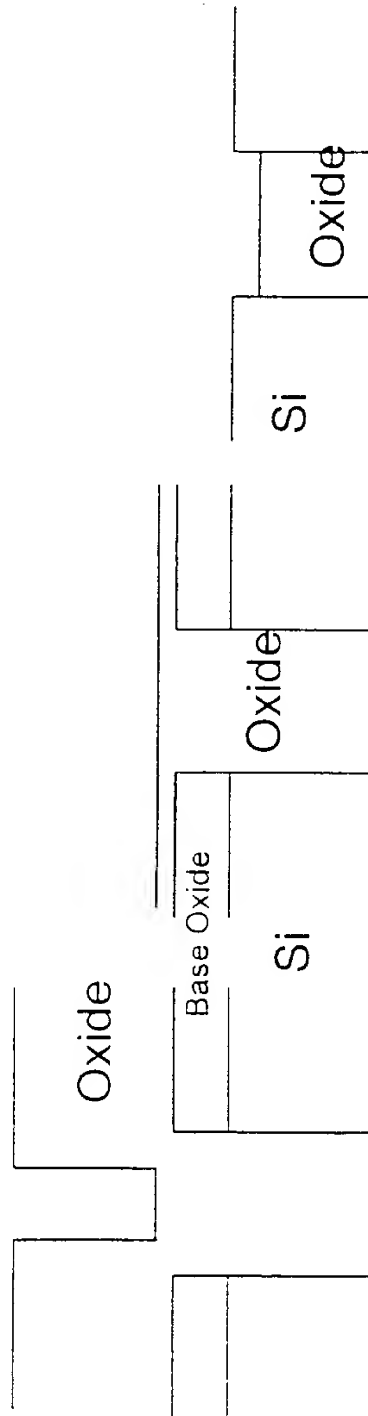


Exhibit A- page 8



CYPRESS

STI Invention Disclosure

Method of Making STI

Option 1

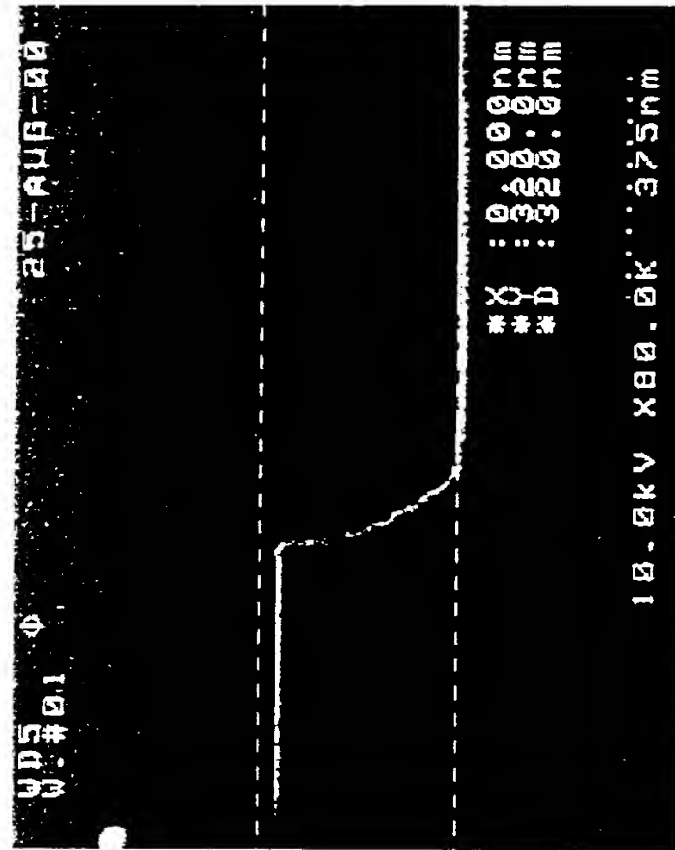
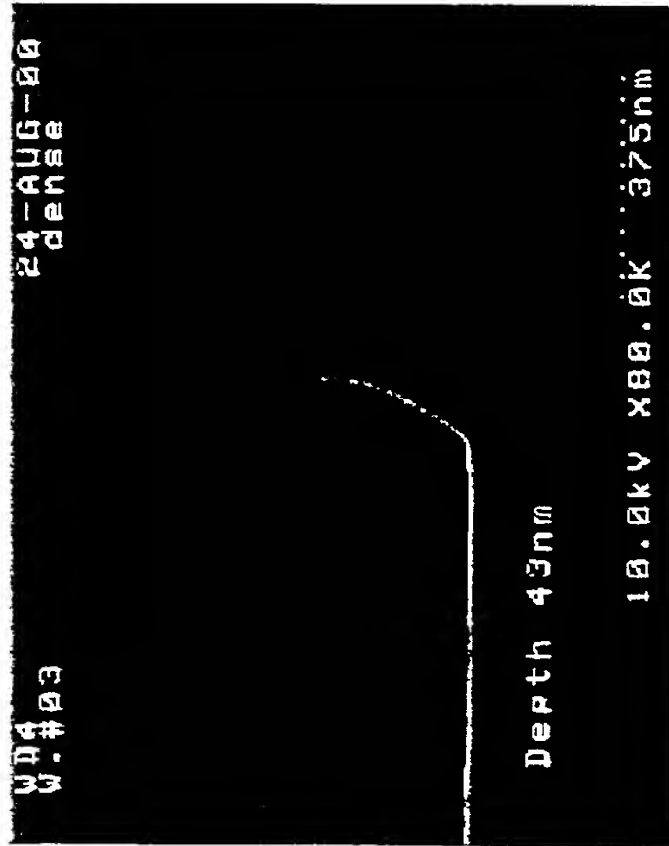


Exhibit A - page 9



CYPRESS

STI Invention Disclosure

Option 2

- Use doped oxide to increase selectivity during wet Dip
- polish to flatness - Fixed Abrasive
- Wet dip - ratio of doped oxide thickness to un-doped thickness controls step height

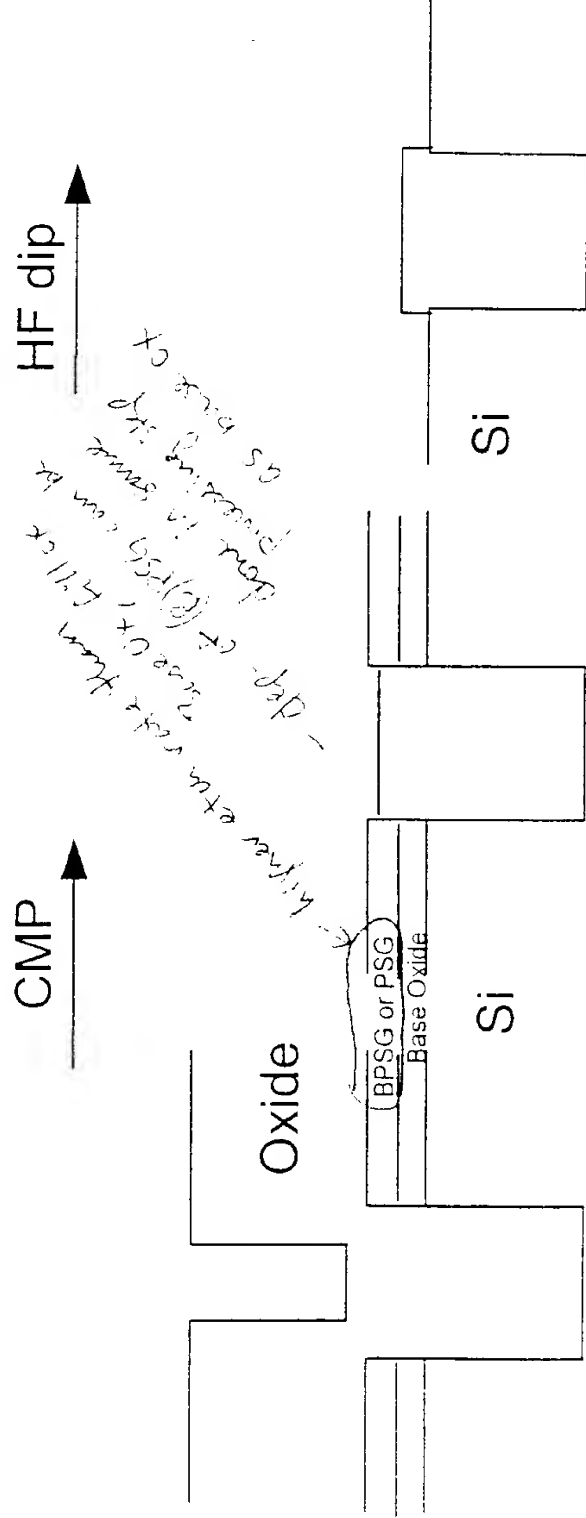


Exhibit A - page 10



CYPRESS

STI Invention Disclosure

Option 3

*10/13 Nitx: fixed (2000 Å) to
act as CMP polish stop*

- Use thin Nitride
- polish to flatness - Fixed Abrasive, stop with oxide over Nitride, nitride is used to determine the step height and not as polish stop.
- Wet dip - Nitride thickness controls step height

CMP

HF dip + Nitride Strip

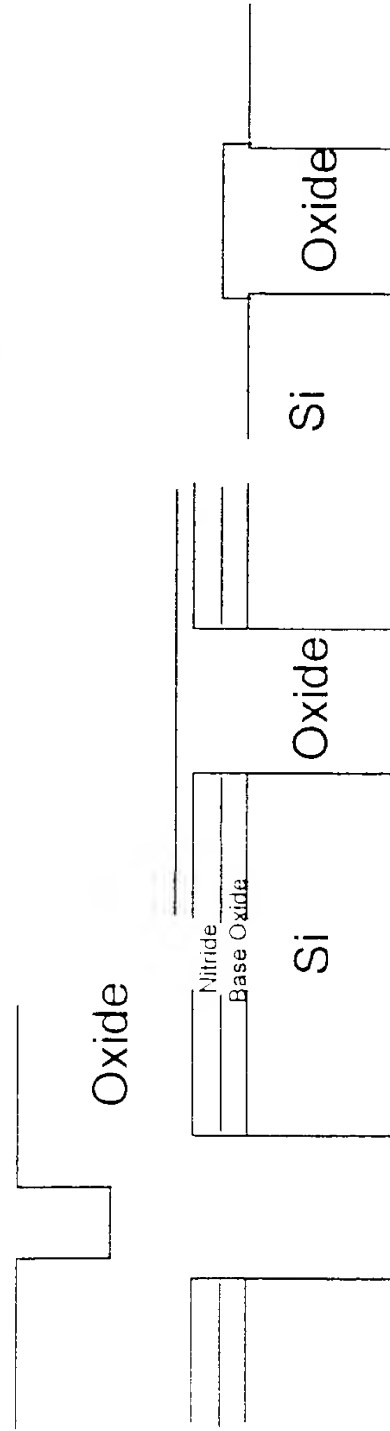
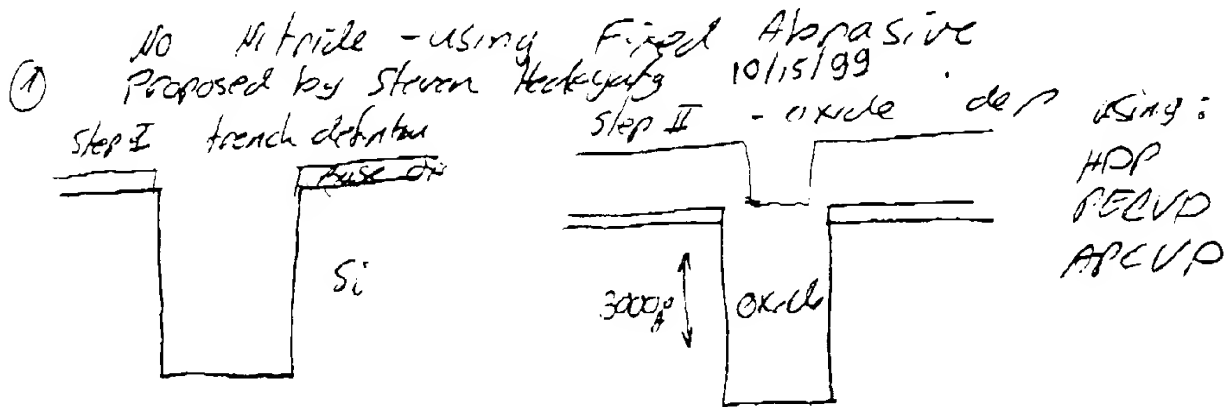


Exhibit A - page 11

STC

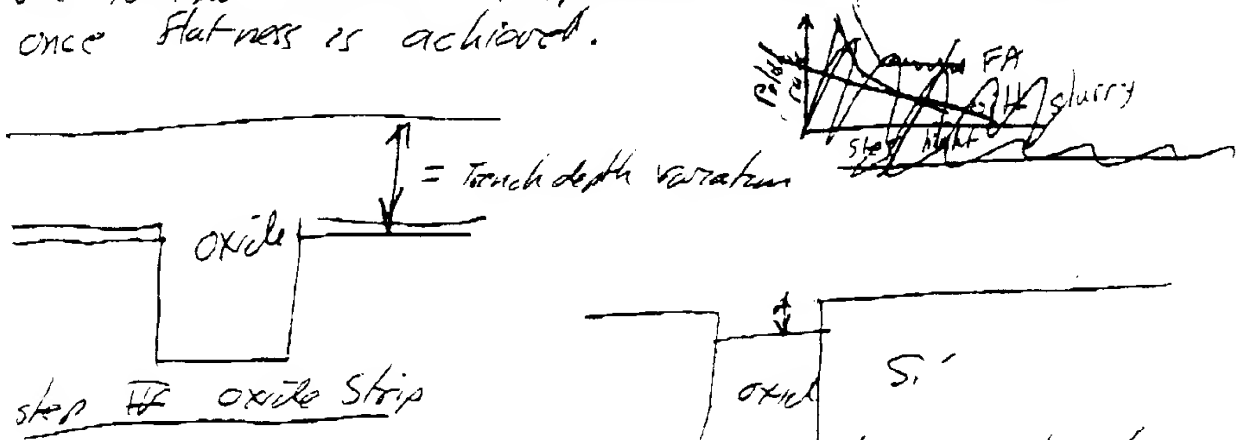
method of making shallow trench isolation
structure with no/or thin nitride cap stop.



in step II
need to deposit trench depth + trench depth variation

step II Oblish

due to Fixed Abrasive properties CMP will self planarize
once flatness is achieved.



Strip will result in oxide below Si level

Steven Hegedus, Ron Kumar, Bill Kating, Mike Allison
S. Hegedus
H. Blossie

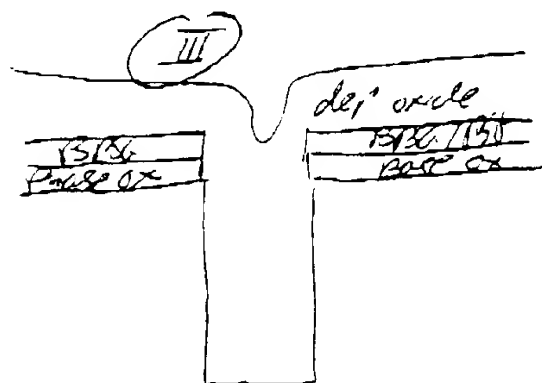
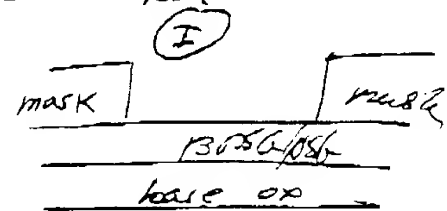
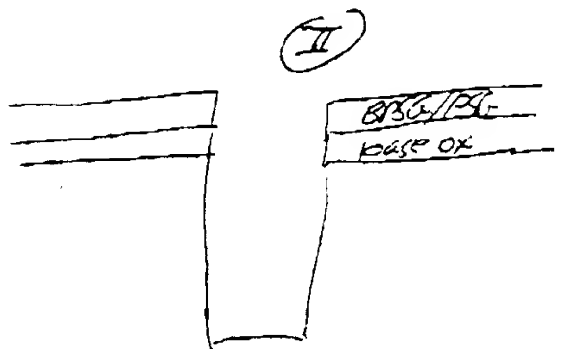
11/15/99
11/15/99

Exhibit B - page 1

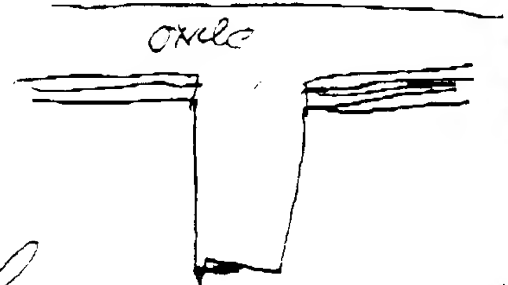
STC

as long as trench depth variation is controlled below a certain number ie $\pm 500 \text{ \AA}$ then polish can be done without ~~the~~ nitride layer.

(2) 2nd method use of ps/psg layer as a base oxide or on top of base oxide



(IV)
Polish using Fixed Abrasive

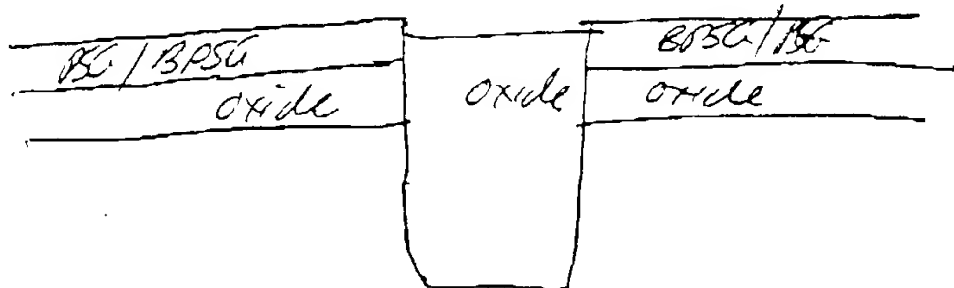


Bill Koutney R.K. M
S. Hedgeli
Alan Blore

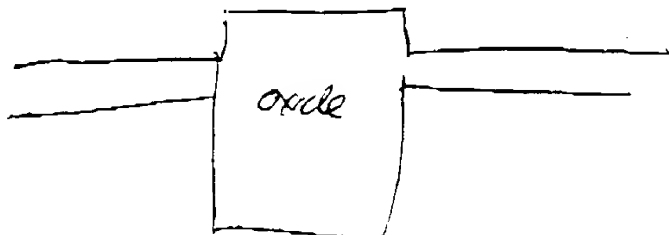
11/15/89
11/15/89

Exhibit B- page 2

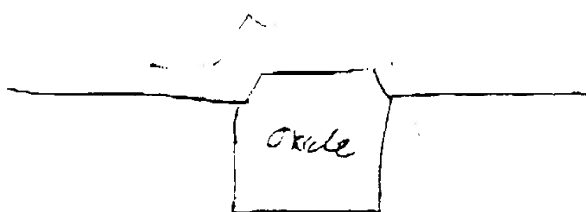
~~strip oxide back to BPSG~~
 Polish Back to BPSG layer
 strip



use wet strip BPSG ER is N 50 time
 thermal oxide rate so result will be
 after strip I



after strip II



BH Kouras 1/26 C/Lha
 J. Hedysle
 DA. 1/26

11/15/89
 11/15/90

Exhibit B - page 3

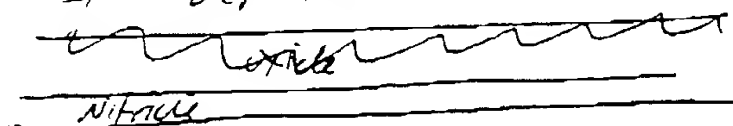
Si

(3)

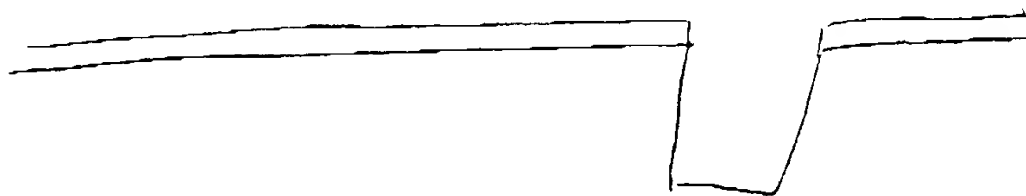
use thin Nitride for Si

Nitride is used only as a means
to determine oxide height above Si

I dep thin Nitride

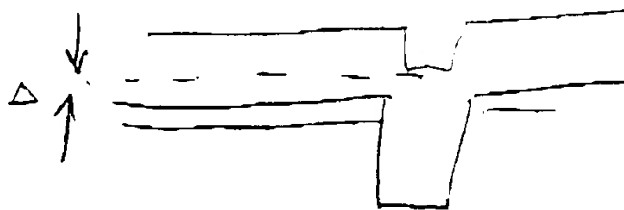


II mask and etch



III

dep HDP oxide or PECVD oxide or APCVD
oxide



Thickness is
targeted to
achieve planarity
at ΔA above

Si

Bill Kautz - 1/15/99

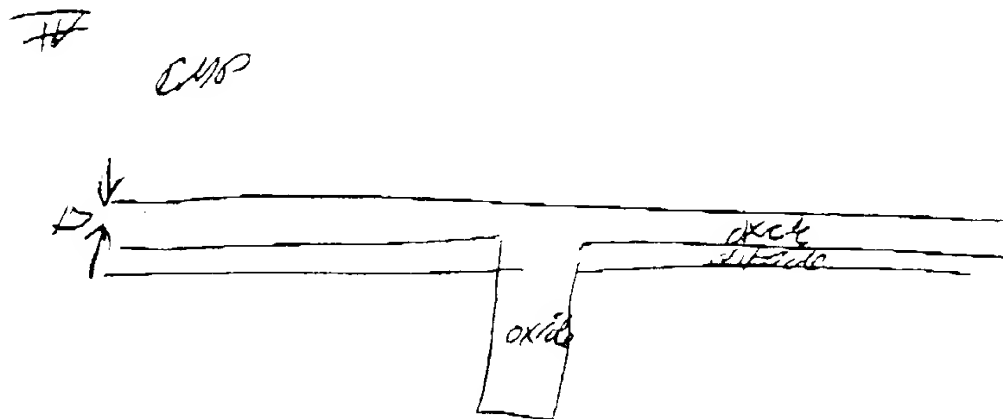
S. Hedgcock

Alan Bloome

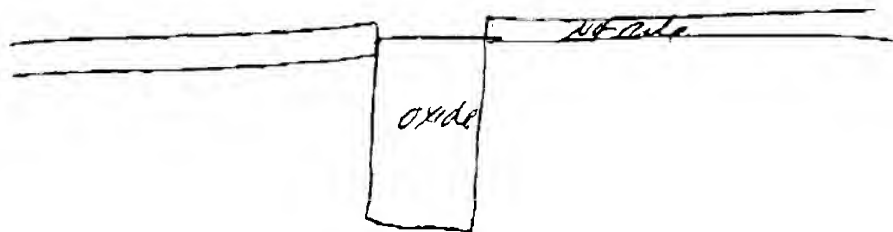
11/15/99

11/15/99

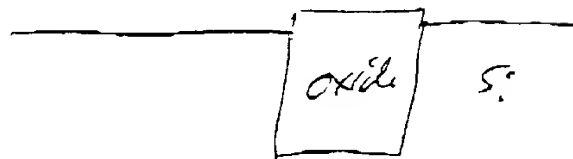
Exhibit B- page 4



IV wet strip of oxide



V pit hole strip



Bill Keweenaw 1/16 6/1/2003
 S. Hedger
 Alami Blom

10/15/89
 10/15/99

Exhibit B - page 5